

## Response to Phosphorus Gettering of Different Regions of Cast Multicrystalline Silicon Ingots

D. Macdonald, A. Cuevas, C. Samundsett and F. Ferrazza\*

Dept. of Engineering, FEIT, Australian National University, Canberra ACT 0200  
Telephone: 61-02-62490078; e-mail: daniel@faceng.anu.edu.au; fax: 61-02-62490506

\* Eurosolare S.p.A. Via A. D'Andrea 6, 00048 Nettuno Italy

### Abstract

Minority carrier lifetimes were measured to determine the effect of phosphorus gettering on cast multicrystalline silicon substrates from central and end regions of two different ingots. One ingot exhibited visibly inferior crystallographic structure, and consistently showed lower lifetimes. For the low quality ingot, wafers from the bottom region did not respond to gettering, whilst those from the top experienced a noticeable lifetime increase. The standard ingot improved markedly at the bottom, but not at all at the top. However, novel cross-contamination experiments showed that *all* top and bottom wafers contained high concentrations of mobile impurities in comparison to central regions. Defect etching revealed that the top and bottom wafers whose lifetime did not increase with gettering had very high dislocation densities, whereas those with low dislocation densities improved markedly after gettering. For the case of the highly dislocated samples, a sufficient number of recombination centres remain to prevent an increase in the lifetime, even after the mobile impurities have been extracted through gettering. Wafers from central regions had moderate dislocation densities and low concentrations of out-diffusible impurities. Their lifetimes increased after gettering up to a more evenly distributed limit imposed by the crystallography. The value of this crystallographic limit was found to be ingot dependent.

### 1. Introduction

Increases in minority carrier lifetime in multicrystalline silicon wafers after a phosphorus gettering process are well documented [1,2]. It is also well known that lifetimes before gettering are in general poorer at the top of an ingot due to lost structure and transition metal impurity segregation [3,4]. Previous work has also shown that the bottom of an ingot tends to contain more crystallographic defects and dissolved oxygen, as well as other impurities from the crucible, which consequently affect the lifetime [5,6]. Phosphorus gettering is known to be very effective at removing transition metals from the active regions of silicon devices, so it seems reasonable to expect that wafers from the top of an ingot would have higher lifetimes after gettering.

However, Sopori et. al. and others have found that gettering is not effective when the dislocation density is above a threshold value of about  $10^6 \text{ cm}^{-2}$  [7]. It has been suggested that in such cases the impurities are precipitated at dislocations, grain boundaries and other microdefects, where they serve to increase the recombination at such centres [8,9].

In order to systematically study the gettering response of wafers from various regions of different quality ingots, we have measured dislocation densities (using a defect etch), and, indirectly, the concentration of ‘mobile’ impurities. This was done using a novel cross-contamination technique, which involved measuring the lifetime degradation of high quality float zone wafers placed very close to the multicrystalline samples during a high temperature step. A proportion of the mobile impurities diffusing out of the surface of the multicrystalline sample will diffuse into the adjacent float zone wafer and consequently degrade its lifetime. The lifetime of the control wafer will thus decrease monotonically with increasing concentration of mobile impurities in the test wafer, allowing ‘dirty’ and ‘clean’ samples to be discriminated in a qualitative way.

Combining the results of the gettering experiments, the defect etching, and the cross-contamination experiments, a clearer picture of the prominent lifetime limiting factors emerges.

## **2. Experimental Methods**

The material used in this study was grown by directional solidification at Eurosolare, SpA. While one of the two ingots examined can be considered of standard quality (ingot 6, average grain size  $\approx 40 \text{ mm}^2$ ), the second suffered from anomalous growth conditions, resulting in generally poor crystallography (ingot 8, average grain size  $\approx 5 \text{ mm}^2$ ). Figure 1 depicts a typical wafer from each ingot, illustrating the difference in crystallography. Sample dimensions are  $50 \times 50 \text{ mm}$ , cut from larger  $100 \times 100 \text{ mm}$  wafers.

Figure 1: Typical ingot 6 wafer (left), and ingot 8 wafer (right).

The resistivity of wafers from each ingot was measured using a contactless induction coupling device. The resistivity was found to decrease from the bottom to the top for both ingots, as expected due to boron segregation, ranging from 0.9 to 0.8  $\Omega\text{cm}$  for the standard ingot, and from 1.5 to 1.0  $\Omega\text{cm}$  for the defective one. Both ingots were p-type.

Four wafers were selected from each of four regions of each ingot in order to examine the dependence of gettering response on ingot position. Region A corresponds to the top of the ingots, region B is 1/6 of the total ingot length below the top, region C is in the centre and region D at the bottom. The total ingot length prior to sawing was 18cm. Under normal industrial conditions the top 3cm are discarded, but for this study they were retained and constitute region A.

Minority carrier lifetimes were measured using the quasi-steady state photoconductance method (QSSPC), which is well suited to multicrystalline silicon [11]. The as-cut wafers had very high surface recombination velocities (effectively infinite), so it was necessary to etch and passivate the surfaces before meaningful lifetime measurements could be taken. Surface passivation was achieved by a light phosphorus diffusion at 840°C using a  $\text{POCl}_3$  source for 25 minutes. A thin oxide layer was then grown at 900°C for 30 minutes (including the last 10 minutes in  $\text{N}_2$ ), followed by a 25 minute forming gas anneal at 400°C. The sheet resistivity of the diffused layer was typically 250  $\Omega/\square$ . Float zone wafers were included in the runs as controls, and measurements of surface recombination in these wafers indicated that the quality of the surface passivation was sufficient to measure lifetimes up to 200 $\mu\text{s}$  in the multicrystalline samples. None of the lifetimes measured for such samples in this study exceeded 50 $\mu\text{s}$ .

After the initial surface passivation the minority carrier lifetimes of the samples were measured using the QSSPC technique. The passivating layers were then etched off and the wafers given a 3 hour 900°C  $\text{POCl}_3$  gettering diffusion, terminated by a 20 minute dry oxidation. The sheet resistivity of the float zone controls after gettering was typically 7 $\Omega/\square$ , with a phosphorus glass layer visible. The heavily diffused layers were then etched off and the wafers repassivated with another light diffusion, identical to the initial process, with another oxide layer formation and forming gas anneal. The lifetimes were then remeasured. After the entire process the wafers were about 40 $\mu\text{m}$  thinner due to the etches, resulting in an average post-getter wafer thickness of around 320 $\mu\text{m}$ . Four samples from each region of each ingot were gettered in a series of four independent experiments (8 samples per experiment). Wafers from each region were split across two experiments to allow results to be compared and confirmed, and care was taken to avoid cross-contamination from ‘dirty’ to ‘clean’ wafers.

Controlled cross-contamination experiments using float zone control wafers were conducted to determine qualitatively the extent of out-diffusion of impurities at high temperatures, and

hence indirectly evaluate the concentration of mobile impurities in the samples. Each multicrystalline sample was 'sandwiched' between two control wafers, which absorb out-diffusing impurities. The distance between the controls and the samples was about 5mm. The control wafer upstream of a sample should receive a lower dose of impurities than the downstream wafer, which is likely to be subjected to impurities on both surfaces due to turbulence in the gas stream. Accordingly, experiments showed that upstream controls had lifetimes 2 to 3 times larger than the downstream controls for sufficiently contaminated samples.

Clearly it is important to avoid impurities from upstream groups of wafers contaminating the controls surrounding other multicrystalline wafers further downstream. To minimise the risk of this happening, the separation between each group of three wafers was kept as large as possible (about 10cm). Also, wafers which were known to contain large amounts of diffusible impurities were placed at the downstream end of the boat. As a result of these measures, contamination from upstream wafers is negligible, as indicated by the lifetimes of the control wafers in front of each sample.

The wafers were given the standard light phosphorus diffusion and oxidation (as described above). This process served the dual purpose of allowing out-diffusion of impurities, and also achieved surface passivation for lifetime measurement.

A second useful application of the cross-contamination effect was employed to determine if the gettering process was complete after the 3 hour heavy phosphorus diffusion. Contaminated control wafers from the first passivating light diffusion and oxidation were included in the post-getter passivating diffusion and oxidation, in order to evaluate the 'cleanliness' of the wafers after the gettering treatment. If the lifetimes of the control wafers recover to near their normal uncontaminated values, then it seems that out-diffusion from the samples ceased at some point, allowing the impurities in the control wafers to out-diffuse. Clean control wafers after the final passivation imply then that gettering was completed.

In addition to the experiments described above, one wafer from each region of each ingot was mechanically polished, chemically cleaned and etched, and then defect etched in Yang's etchant [12]. This defect etch provides good delineation of dislocations for a range of crystal orientations, although like other commonly used etches, it does not effectively etch all orientations [13]. SEM micrographs were taken of suitably etched areas, and dislocation densities calculated for each sample.

### **3. Results and Discussion**

#### **3.1 Dislocation Densities**

Figure 3 gives the dislocation densities for each region of each ingot. These are average values, and it should be noted that in the samples with high dislocation densities there were some regions with values as high as  $10^8 \text{ cm}^{-2}$ . Such regions have been thought responsible for significant lifetime degradation in other studies [13]. Curiously, the distribution of dislocation densities is opposite for the two ingots. This may be a reflection of the anomalous growth conditions that the defective ingot (ingot 8) is suspected to have undergone. Figure 4 shows SEM micrographs of high dislocation density samples.

**Error! Not a valid link.**

Figure 3: Average dislocation densities for both ingots by region.

Figure 4: SEM micrographs of defect etched samples.

### 3.2 Cross-Contamination

The results of the cross-contamination experiments are presented in Table 1 and Figure 5 in the form of lifetimes of the downstream control wafers ( $\tau_{fz}$ ), and a mobile impurity density ranking (MI Density). The downstream wafers are used for analysis because they are least likely to be affected by other wafer batches upstream, and also because they are exposed to a greater dose of impurities from the sample. In an uncontaminated environment, the high resistivity ( $1000 \Omega\text{cm}$ ) control wafers would yield a lifetime of around 4ms under the light phosphorus diffusion conditions. The most heavily contaminating multicrystalline samples degraded the control wafer lifetime to  $100 \mu\text{s}$  in some cases. It is difficult to quantitatively relate the degraded lifetime to the concentration of mobile impurities in the test sample, primarily due to the fact that it is unclear what type of impurities are out-diffusing, and also because of the turbulent effects of the gas flow. It is possible however to discriminate qualitatively between ‘clean’ and ‘dirty’ wafers, which is useful in analysing the gettering results.

**Error! Not a valid link.**

Figure 5: Cross-Contamination Results

Ingot, Region	$\tau_{fz}$ ( $\mu\text{s}$ )	MI Density	Ingot, Region	$\tau_{fz}$ ( $\mu\text{s}$ )	MI Density
6A	280	high	8A	530	moderate
6B	500	moderate	8B	1300	low
6C	3000	very low	8C	3000	very low
6D	175	very high	8D	150	very high

Table 1: Cross-contamination results.

### 3.3 Surface Passivated Non-Gettered Wafers

The lifetime measurements for passivated only (non-gettered) wafers are shown in Figure 6. The surface passivation is of good enough quality to interpret the measured lifetimes as bulk lifetimes, and since the gettering effect of the light diffusion is small, we associate the lifetimes with non-gettered material. Both ingots show very poor lifetimes of about  $1\mu\text{s}$  in both the top and bottom regions. Lifetimes for wafers from 6D and 8A would be expected to improve after gettering due to the low dislocation densities and high levels of out diffusion. However, the high dislocation densities of 6A and 8D suggest that their lifetimes are limited by dislocations and other defects which may be decorated with impurities. Consequently their lifetimes are not expected to increase, irrespective of the high concentration of mobile impurities.

**Error! Not a valid link.**

Figure 6: Lifetimes of Passivated Wafers

Wafers from region B had average values of  $16\mu\text{s}$  and  $8\mu\text{s}$  for ingots 6 and 8 respectively, while region C had the highest lifetimes with averages of  $32\mu\text{s}$  and  $11\mu\text{s}$  for the two ingots, respectively. Interestingly, the grain structure of B and C region wafers of each ingot appear very similar, and they also have similar dislocation densities. The cross-contamination results show that B region wafers have a higher concentration of mobile impurities, which fits with the fact that region B is located closer to the top of the ingot, and hence would supposedly contain more transition metal impurities. These three facts taken together suggest that region B wafers should respond to gettering, since the crystallography seems no worse than for region C. It is possible that region C wafers will also respond to gettering, although it is unclear at this stage if the lifetime is limited by impurities or structural defects.

QSSPC lifetime measurements allow an implied  $V_{oc}$  to be determined from the variation of lifetime with carrier density [11]. Using this technique, a lifetime of  $32\mu\text{s}$  should allow for open circuit voltages of up to  $640\text{mV}$  for ingot 6. Bearing in mind the higher resistivity (lower doping) of ingot 8,  $11\mu\text{s}$  is a relatively low lifetime, alluding to the poor crystallography of the ingot. The maximum achievable voltage for ingot 8 is in the vicinity of  $600\text{mV}$ .

### 3.4 Gettered Wafers

**Error! Not a valid link.**

Figure 7: Ingot 6 Passivated and Gettered Lifetimes

Figure 7 shows the effect of gettering on ingot 6 wafers. Lifetimes for wafers from region A (top) have not increased by any measurable amount. The dislocation density of such wafers was measured as  $10^7$ , which is well above the suggested threshold value of  $10^6\text{ cm}^{-2}$ . Interestingly, these wafers exhibit high concentrations of mobile impurities. A simple model of impurity behaviour might suggest that highly dislocated samples would contain most of

their impurities in a precipitated state. Previous work has shown that such ‘trapped’ impurities are not easily getterable [10]. Consequently, high dislocation density wafers might be expected to exhibit relatively low mobility of impurities at standard processing temperatures, resulting in low out-diffusion. We find that this is not the case for highly dislocated wafers from both the top and bottom of an ingot. In fact the out-diffusion of mobile impurities does not seem to depend strongly on the dislocation density. We have not been able to determine whether the out-diffusing impurities are coming from precipitated states at dislocations, grain boundaries or microdefects, or from the bulk of the grains. In any case, it seems that their effect on the recombination strength of such sites is small, and these mobile impurities are in a sense ‘surplus’.

Region B of ingot 6 showed an improvement of 160% to  $41\mu\text{s}$ , bringing it up to a similar level as region C (up by 25% to  $39\mu\text{s}$ ). This is consistent with the reasoning above, which suggested that B region wafers should improve to the level of the C region. The C region wafers have a relatively low concentration of mobile impurities, the removal of which has resulted in the small lifetime increase. It is expected that the lifetime in these gettered wafers is limited by crystallographic defects such as dislocations (which occur in moderate density), grain boundaries, and other microdefects which could not be observed with the defect etch used here [8,9,13].

Region D (bottom) exhibits an 8-fold increase to about  $20\mu\text{s}$  for ingot 6, which seems feasible considering the low dislocation density. In this case it is clear that the ungettered wafers are limited by the presence of mobile impurities, which are present in large concentrations (table 1). It is worthwhile noting that these region D wafers would be suitable for cell fabrication after a gettering step, whereas without one, such wafers would normally be discarded. Using the implied voltage technique described above, an increase in lifetime from  $1\mu\text{s}$  to  $20\mu\text{s}$  corresponds to a voltage increase of 590mV to 630mV, approximately.

Figure 8: Ingot 8 Passivated and Gettered Lifetimes

**Error! Not a valid link.**

Figure 8 depicts the gettering results for ingot 8. Region A has improved 4-fold to around  $4\mu\text{s}$ . An increase is consistent with the low dislocation density, and once again the lifetime is limited by the crystallography. As was the case for ingot 6, region B has increased to a level similar to region C (about  $11\mu\text{s}$ ), although in this case the increase in region C wafers is very small.

Region D wafers from ingot 8 did not improve after gettering. These samples had the largest grain size of all the wafers (even compared with ingot 6), and yet displayed the lowest lifetimes after gettering. The low lifetime is predicted by the high dislocation density, which is well above the threshold suggested by Sopori et. al. [7]. As mentioned in section 2, control wafers were included in the post-getter passivating diffusion in order to determine if out-diffusion had ceased, thus implying that gettering was completed. These controls recovered to lifetimes of around 3ms, indicating that out-diffusion had indeed ceased during the 3 hour

heavy diffusion for samples from all regions. Hence 8D and 6A wafers (no lifetime increase) are in fact ‘clean’ (very few mobile impurities) after the gettering step, although there is likely to be some (possibly many) impurities precipitated at defects. The low lifetimes of these samples are caused by the high concentration of defects and the non-getterable impurities decorating them.

Although the central regions of ingot 8 follow the same trends as ingot 6, the lifetimes are consistently lower. This is attributable to the poorer grain structure, and presumably higher density of microdefects, that resulted from the perturbed growth of the ingot.

## Conclusions

The largest increase in lifetime after phosphorus gettering was found in samples with low dislocation densities and high concentrations of mobile (and hence getterable) impurities. The lifetime of samples with dislocation densities above  $10^6$  remained low after gettering, despite their high initial concentration of mobile impurities, implying that the presence of dislocations does not excessively impede the ability of gettering to remove certain impurities. It is possible that the dislocations and microdefects in such samples are saturated with impurities, and those found out-diffusing are ‘surplus’. Consequently, their removal does not affect the lifetime.

The lifetime response to phosphorus gettering was also found to be ingot dependent. The low quality ingot had a modest lifetime increase in the central regions (to  $11\mu\text{s}$ ), whilst the top region also increased to  $4\mu\text{s}$ . The standard ingot improved in the central regions (to  $41\mu\text{s}$ ), especially off-centre (region B). Hence gettering may be a viable option for improving cell efficiencies for substrates from such off-centre regions. The standard ingot also improved markedly at the bottom of the ingot ( $20\mu\text{s}$ ). Considering that such wafers are normally discarded, gettering seems to be an excellent option for salvaging them and fabricating good quality cells.

Lifetimes in the central regions of both ingots improved with gettering, but reached an upper limit which was approximately constant along the central part of the length of the ingots. This underlying crystallographic limit was higher for the standard ingot, and is most likely due to the presence of decorated dislocations (which were present in moderate densities in such regions), grain boundaries, and other microdefects.

## References

1. J. S. Kang, D. K. Schroder *J. Appl. Phys.* 65 (8) 2974 (1989)
2. A. Cuevas, M. Stocks, S. Armand, M. Stuckings, *App Phys Lett* 70 (8) 1017 (1997)
3. A. Laugier, E. Borne, H. El Omari, G. Goer, D. Sarti, *Proc. 25th IEE PVSC* 609 (1996)
4. F. Ferrazza *POLYSE '95* \*

5. M. Ghosh, D. Yang, A. Lawrenz, S. Riedel, H. Möller, *Proc. 14th Europ. PVSEC* Vol 1 724 (1997)
6. G. Goaer, D. Sarti, B. Paya, K. Mahfoud, J. Muller, *Proc. 14th Europ. PVSEC* Vol 1 845 (1997)
7. B. L. Sopori, L. Jastrzebski, T. Tan, *Proc. 25th IEEE PVSC* 625 (1996)
8. M. Werner, E. Weber *Proc. 24th IEEE PVSC* 1611 (1994)
9. S. McHugo, J. Bailey, H. Hieslmair, E. Weber, *Proc. 24th IEEE PVSC* 1607 (1994)
10. S. McHugo, H. Hieslmair, E. Weber, *Mat. Sci. Forum*, 196-201 1979 (1995)
11. R. Sinton, A. Cuevas, *Appl. Phys. Lett.* 69 (17) 2510 (1996)
12. K. H. Yang, *J. Electrochem. Soc.* 1140 (May 1984) \*
13. H. J. Möller, *Solid State Phenomena* 47-48 127 (1996)