Towards industrial advanced front-junction *n*-type silicon solar cells

Yimao Wan[1], Chris Samundsett[1], Teng Kho[1], Josephine McKeon[1], Lachlan Black[1], Daniel Macdonald[1], Andres Cuevas[1], Jian Sheng[2], Yun Sheng[2], Shengzhao Yuan[2], Chun Zhang[2], Zhiqiang Feng[2] and Pierre J. Verlinden[2]

[1]Research School of Engineering, The Australian National University, Canberra, ACT 0200 Australia

[2]State Key Lab of PV Science and Technology, Trina Solar Limited, No. 2 Trina Road, Trina PV Park, New District, Changzhou, Jiangsu, China 213031 China

***ABSTRACT* — Recent progress in the development of advanced front-junction *n*-type monocrystalline solar cells for potential industrial fabrication is presented. The textured, boron-diffused front surface is passivated with a stack of Atmospheric Pressure Chemical Vapor Deposited (APCVD) Al_2O_3 and Plasma-Enhanced Chemical Vapor Deposited (PECVD) SiN_x. A champion cell with an in-house measured efficiency of 21.6% is obtained for small-area cells (i.e., 2×2 cm^2) fabricated at the ANU. The high open-circuit voltage of 664 mV demonstrates the excellent passivation of both the front and rear surfaces. The cell design and process have demonstrated a good tolerance to substrate resistivity variations, with an average cell efficiencies close to 21% for resistivity varying between 3 and 10 Ω·cm. Moreover, with an adaption of the process developed at the ANU, large-area cells (i.e., 12.5×12.5 cm^2) are fabricated at Trina Solar on *n*-type Cz substrates with a resistivity of 2.5 Ω·cm. A champion cell with an in-house measured efficiency of 20.5% is obtained, demonstrating a high potential in commercializing the advanced cells developed in this work. Finally, simulations reveal that further improvements in cell efficiency are to be mainly achieved through further optimisations of the rear side contact geometry and rear surface passivation.**

***Index Terms* — silicon, surface passivation, boron, phosphorus, photovoltaic cells.**

I. Introduction

P-type silicon solar cells are still the workhorse for industrial crystalline silicon solar cell manufacturing. However, as the silicon PV industry moves to introduce advanced high-efficiency solar cell concepts, the quality of the base material is becoming more and more important [1]. The high oxygen content in the standard *p*-type Czochralski (Cz) silicon reacts with the boron dopant under illumination and degrades the cell performance, a process known as light-induced degradation (LID) [2, 3]. *N*-type wafers do not suffer from LID, and also feature a higher tolerance to common metal impurities such as Fe, resulting in higher minority carrier diffusion lengths compared to *p*-type counterparts [2, 4]. *N*-type wafers therefore have a better material quality, even if made by the Cz method, which allows the full potential of high-efficiency cell designs to be realized.

Starting from common designs that have a dopant diffusion of opposite polarity on each of the two surfaces of the wafer, the next step towards higher efficiency is to passivate not only the front but also the back surface, which commonly requires the localized, or partial formation of the rear metal contact [5]. A key feature in the high efficiency front-junction cell is the passivation of the boron-diffused front surface, which has historically been a major challenge in the PV industry, but has recently become more feasible by using the negatively charged dielectric aluminum oxide (Al_2O_3). This dielectric layer has been proven to provide excellent surface passivation of p^+-diffused surfaces [6], even after a typical firing process [7-9]. While initial work was mostly based on atomic layer deposition (ALD) [10, 11], deposition of such highly-passivating films has since been demonstrated via several high-throughput techniques, including spatial ALD, plasma-enhanced chemical vapour deposition (PECVD), atmospheric pressure chemical vapour deposition (APCVD), and reactive sputtering.

Another feature in this architecture is the application of a dielectric layer on the fully phosphorus-diffused rear side, allowing both an improvement in rear side reflectance, as well as improved rear side passivation. An obvious choice for this film is PECVD silicon nitride (SiN_x), which has been demonstrated to provide good passivation of n^+-diffused surfaces [12, 13].

In this contribution the applicability of APCVD Al_2O_3 / PECVD SiN_x stacks for passivation of front p^+-diffused surfaces, and PECVD SiN_x for rear n^+-diffused surfaces are investigated. The deposition of Al_2O_3 by APCVD is of great interest because of its relative simplicity and high throughput compared to other deposition techniques [14]. The effects of *(i)* silicon base resistivity, and *(ii)* rear contact geometry, on solar cell performance are studied, both experimentally on small area cells, and via modelling. Initial results on large-area cells fabricated at Trina Solar are also reported.

II. Cell structure

Fig. 1 depicts the *n*-type solar cell structure with two homogeneous full-area diffusions and a partial rear contact.

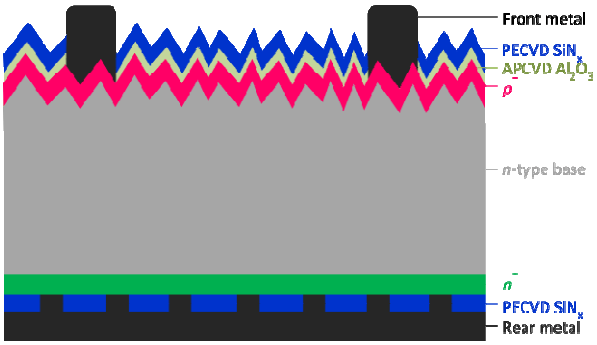

Fig. 1: Schematic cross-section of a high efficiency front-junction *n*-type silicon solar cell.

III. Results and Discussion

A. Passivation of front p^+ and rear n^+ diffused surfaces

Fig. 2 presents the experimental results of passivation of Si surfaces that are relevant to this work: the front surfaces with textured boron diffusion, and the rear surface with planar phosphorus diffusion.

Reports on the passivation of textured p^+-diffused surfaces by deposited dielectrics are relatively rare in the literature. Using Al_2O_3/SiN_x dielectric stacks deposited in an industrial inline PECVD, Duttagupta *et al.* [15] obtained relatively low saturation current densities (J_{0p+}) on boron diffused textured surfaces with sheet resistance ranging from 30 to 180 Ω/□. Note that the required thermal activation of the Al_2O_3 films was performed in a standard industrial fast-firing furnace, making the developed passivation stack industrially viable. Upon passivation with the PECVD a-Si/SiN_x stack, Kessler *et al.* [16] attained comparable passivation quality on boron diffused textured surfaces with sheet resistances ranging from 60 to 550 Ω/□. They also demonstrated the passivation stack was thermally stable up to 600 °C for 60 minutes. Furthermore, we also note that the lowest J_{0p+} measured on a 550 Ω/□ boron-diffused textured region is 3.5 fA/cm^2. The front textured p^+ surface featured in our cells has a sheet resistance of 110 Ω/□ and is passivated by an APCVD Al_2O_3/ PECVD SiN_x stack, possessing a J_{0p+} of 25 fA/cm^2, which is comparable to the state of the art passivation quality.

Several previous works studied the passivation of planar n^+ surfaces, with the best surface passivation obtained by Kerr *et al.* [12] using aluminum annealed (alnealed) thermal SiO_2. Recently, we have developed a unique PECVD SiN_x that is lowly-absorbing and highly-passivating [13], as evident in Fig. 2. A J_{0n+} of 52 fA/cm^2 is achieved on a symmetrically SiN_x-passivated planar n^+ diffused control sample with a sheet resistance of 100 Ω/□.

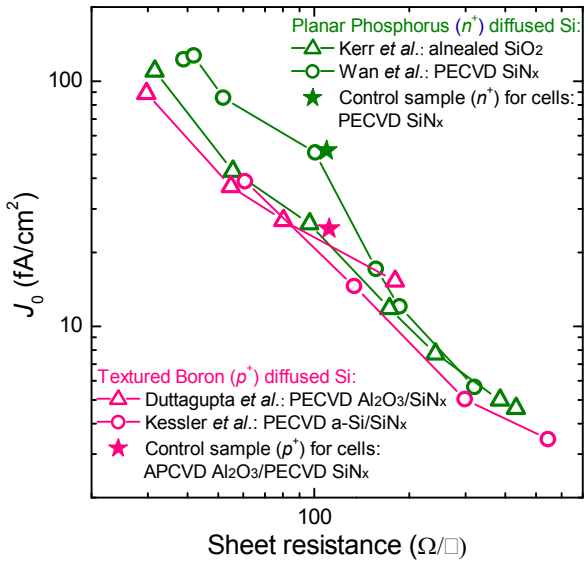

Fig. 2: Effect of sheet resistance on the J_0 of boron (p^+) diffused textured surfaces, and on the J_0 of phosphorus (n^+) diffused planar surfaces. The results from Duttagupta *et al.* [15], Kessler *et al.* [16], Kerr *et al.* [12] and Wan *et al.* [13] are included for references.

B. Effect of wafer resistivity

An often-mentioned challenge for the industrial development of *n*-type cells arises from the larger segregation coefficient of phosphorus in the Cz crystal growth process [17]. While boron-doped crystals typically have a resistivity spread of a factor of 2-3, the spread for *n*-type crystals is approximately a factor of 6-10. To avoid any negative impact of this variation on cell performance it is necessary to ensure that the device design is able to cope with a significant spread in wafer resistivity.

Fig. 3 presents the cell parameters as a function of base resistivity that ranges from 3 Ω·cm to 10 Ω·cm for a batch of 2×2 cm^2 cells fabricated at the ANU. Among a total of 57 cells measured (i.e., 20 cells with 3 Ω·cm, 19 cells with 5 Ω·cm and 18 cells with 10 Ω·cm), 27 of these cells had efficiencies above 21% and only 1 cell was below 20% (i.e., 19.96%).

TABLE I: Summary of Cell Results

Base (Ω·cm)		V_{oc} (mV)	J_{sc} (mA/cm^2)	*FF* (%)	η (%)	Area (cm^2)
3	Average	661	40.0	80.4	21.1	2×2[#]
(20 cells)	Best	664	40.2	81.2	21.6	
5	Average	657	40.2	80.0	21.0	
(19 cells)	Best	664	40.4	80.9	21.6	
10	Average	651	40.3	79.2	20.7	
(18 cells)	Best	655	40.4	79.8	21.0	
2.5	Average	660	39.4	77.2	20.1	12.5×
(4 cells)	Best	658	39.8	78.3	20.5	12.5*

[#]: Fabricated at the ANU
*: Fabricated at Trina Solar

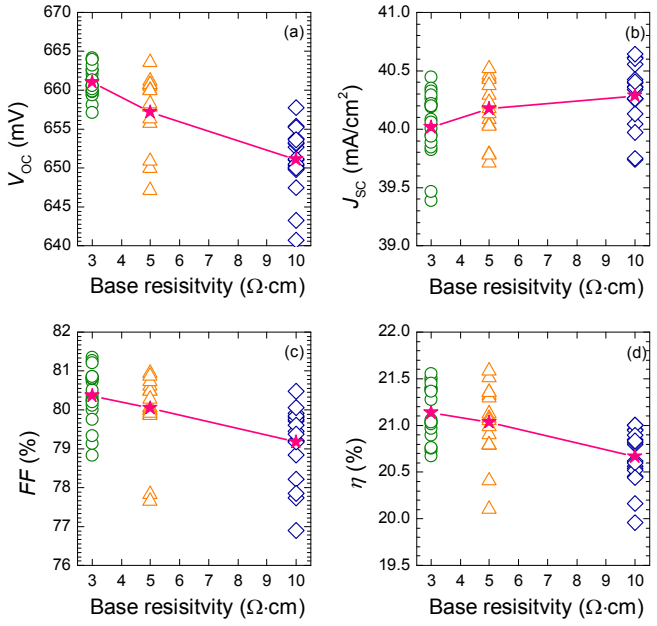

Fig. 3: Effect of base resistivity on small area cell parameters (a) V_{OC}, (b) J_{SC}, (c) *FF*, and (d) efficiency η. The average is indicated in red stars.

The results clearly show that V_{OC} is highest for 3 Ω·cm wafers; this is consistent with the fact that device voltage is directly related the product of electron and hole concentrations *pn*, with a lower resistivity helping via a higher majority carrier concentration. J_{SC} is highest for 10 Ω·cm, as expected due to greater carrier diffusion length. *FF* is higher for lower resistivity, indicating that the same reasons that lead to a higher V_{OC} also apply to V_{mp}, and possibly due also to some impact of lateral resistive losses in the base. The resulting efficiency is highest for 3 Ω·cm, revealing that the benefits in V_{OC} and *FF* outweigh the small loss in J_{SC}. Given the fact that both V_{OC} and *FF* should be better in even lower resistivity material, it is quite likely that wafers with resistivity < 3 Ω·cm can in fact give better cell performance using this cell structure, provided there is not a large reduction in bulk lifetime. The highest V_{OC} obtained in this work, 664 mV, demonstrates excellent passivation of both front p^+ and rear n^+ surfaces, even if there is further room for improvement.

Above those small differences, the clear conclusion is that this cell process has a good tolerance to resistivity variations, with average cell efficiencies close to 21% for resistivity between 3 and 10 Ω·cm, and probably also for even lower resistivity. Substrates with lower resistivity are also being investigated and the results will be reported at the conference.

Finally, with an adaption of the process developed at the ANU, large-area cells (i.e., 12.5×12.5 cm^2) were fabricated at Trina Solar on *n*-type Cz substrates with a resistivity of 2.5 Ω·cm. As presented in Table I, a champion cell with an in-house measured efficiency of 20.5% was obtained, demonstrating a high potential in commercializing the cell design and process presented in this work.

C. Modeling of rear contact geometry for further improvement

The effect of the rear contact geometry on cell performance is simulated using the device simulator Quokka [18].

The results depicted in Fig. 4 show that the achievable efficiency is strongly dependent on the sheet resistance and recombination current density of the rear side diffusion, indicating that quite a light diffusion is necessary for >22% across all resistivities. On the other hand, a small compromise in efficiency, down to 21.8%, makes the design more robust, and weakly dependent on the separation between the point contacts.

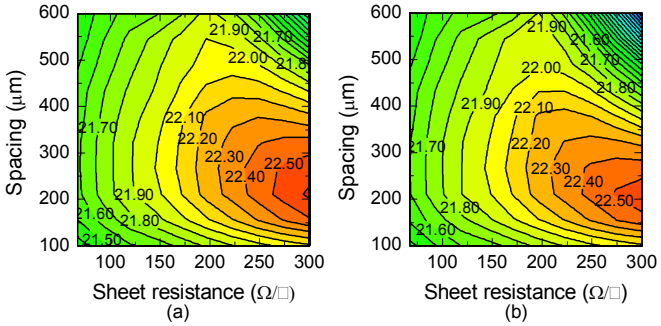

Fig. 4: Contour plot of efficiency as a function of rear dot spacing and rear side sheet resistance for a base resistivity of (a) 3 Ω·cm, and (b) 10 Ω·cm. The dot size is 40 μm.

IV. Conclusion

Progress in the development of high efficiency front-junction *n*-type solar cells following simple processes compatible with industrial fabrication is presented. Champion cells with an efficiency of 21.6% for small area (i.e., 2×2 cm^2) and of 20.3% for large area (i.e., 12.5×12.5 cm^2) were demonstrated. The highest V_{OC} of 664 mV demonstrated very good passivation of both the front and rear surfaces. The cell design and process have demonstrated a good tolerance to resistivity variations, with average cell efficiencies close to 21% for resistivity between 3 and 10 Ω·cm, and probably also for even lower resistivity. Finally, simulations revealed the potential for further improvements in cell efficiency through further optimised rear side contact geometry and passivation quality.

Acknowledgements

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