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Investigation of reactive ion etching of dielectrics and Si in CHF_3/O_2 or CHF_3/Ar for photovoltaic applications

C. Gatzert,[a] A. W. Blakers, and Prakash N. K. Deenapanray[b]
Centre for Sustainable Energy Systems, Faculty of Engineering and Information Technology, The Australian National University, Canberra, Australian Capital Territory 0200, Australia

D. Macdonald[c]
Department of Engineering, Faculty of Engineering and Information Technology, The Australian National University, Canberra, Australian Capital Territory 0200, Australia

F. D. Auret
Department of Physics, University of Pretoria, Pretoria 0002, South Africa

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Using a combination of etch rate, photoconductance, and deep level transient spectroscopy (DLTS) measurements, the authors have investigated the use of reactive ion etching (RIE) of dielectrics and Si in CHF_3/O_2 and CHF_3/Ar plasmas for photovoltaic applications. The radio frequency power (rf-power) and gas flow rate dependencies have shown that the addition of either O_2 or Ar to CHF_3 can be used effectively to change the etch selectivity between SiO_2 and Si_3N_4. The effective carrier lifetime of samples degraded upon exposure to a CHF_3-based plasma, reflecting the introduction of recombination centers in the near-surface region. The extent of minority carrier lifetime degradation was similar in both types of plasmas, suggesting that the same defects were responsible for the increased recombination. However, the rf-power dependence of lifetime degradation in *n*- and *p*-type Si was different. Moreover, the lifetime degradation did not exhibit a linear rf-power dependence, suggesting that primary defects were not the dominant recombination centers responsible for the decrease in lifetime. Indeed, DLTS measurements have shown that secondary defects were formed in samples exposed to the plasma after annealing at 400 °C, the temperature at which a SiN:H layer is deposited on samples to passivate their surfaces. The minority carrier lifetime degradation in RIE processed samples could be partially avoided using post-RIE chemical treatments. © *2006 American Vacuum Society.* [DOI: 10.1116/1.2333571]

I. INTRODUCTION

Plasma (or dry) etching has become a dominant technique in semiconductor processing because it provides high-throughput anisotropic etch profiles with good selectivity, which now allow precision transfer of resist patterns with feature sizes below 100 nm.[1] However, there is one area of semiconductor device processing, namely, the fabrication of solar cells, where plasma etching has not made significant inroads. The fabrication of both industrial and laboratory silicon solar cells is still heavily reliant on wet chemical etching and substitution of some or all of the wet chemical steps by dry etching would provide advantages of reduced environmental impact and better safety in the workplace.

Nevertheless, there are a few niche applications in the fabrication of laboratory solar cells where plasma etching has recently been used or investigated. Schaefer and Ludeman have demonstrated a nearly damage-free dry etching process for solar cell processing, whereby dry-processed solar cells showed the same performance as wet etched cells.[2] That study replaced all wet chemical steps by etching in an electron-cyclotron-resonance (ECR) plasma reactor using a combination of SF_6 and CHF_3 chemistries.[2] The same group had previously fabricated Si solar cells with efficiencies up to 17% using a combination of ECR plasma and wet chemical processing, where the latter was used only for metallization.[3] Gazuz *et al.* have recently demonstrated the feasibility of large area silicon solar cell processing using plasma etching.[4] They reported a device efficiency of 14.7% for completely dry-processed cells compared to 15.1% for a wet-processed reference cell. These results are very encouraging regarding the viability of dry etching in the fabrication of solar cells. Other applications of plasma etching in the fabrication of solar cells include the formation of buried base contacts,[5] etching of phosphorous silicate glass,[3,4,6] and texturing.[7,8]

The need to increase the price competitiveness of photovoltaics (PV) relative to nonrenewable energy sources calls for new concepts in solar cell design and fabrication. Typically, a combination of lowering the cost of production of solar cells and modules, and increasing the efficiency of devices has to be used to achieve this aim. In response to this challenge, the group at the Australian National University has developed an innovative low-cost, high-efficiency Si solar cell and the attendant cell assembly technology.[9] The thin-film crystalline Si solar cell is fabricated using a combination of micromachining and conventional solar cell processing. Each cell is typically 50 μm thick and 1–2 mm

[a]Present address: Institut für Physikalische Elektronik, Pfaffenwaldring 47, D-70569 Stuttgart, Germany.
[b]Electronic mail: prakash.deenapanray@anu.edu.au
[c]Electronic mail: daniel.macdonald@anu.edu.au

wide. Among the innovative features of the new cells are (1) the improved Si utilization by a factor ~12, (2) a reduction in the number of wafers per kilowatts by ~30, (3) high efficiency, (4) perfect bifacial response, and (5) high power-to-weight ratio. Reactive ion etching (RIE), in conjunction with wet processing, is used in the micromachining and metallization steps of these solar cells. The number of steps in our current process could be reduced by elimination of a few chemical etch steps by etching dielectric layers (SiO_2 and Si_3N_4) through to the Si substrate. This is desirable for reducing device fabrication complexity and to minimize the use of toxic hydrofluoric acid. Because of the unconventional structure of the thin-film cells, a streamlined fabrication process will be favored by the ability to reverse the etch selectivity between SiO_2 and Si_3N_4 for different steps in the fabrication process.

RIE proceeds via a combination of physical sputtering and gasification of the exposed semiconductor surface. The effect of ion-bombardment-enhanced chemical etching of Si has been elegantly demonstrated by Coburn and Winters more than three decades ago.[10] RIE of semiconductor surfaces involves the two competing processes of damage creation in the near-surface region of the surface exposed to low-energy ion bombardment and the simultaneous removal of part of the damaged layer by etching. The buildup of damage below the surface of the reactive ion etched semiconductor depends on defect introduction rates, dynamic annealing effects, and the diffusion of defects away from the surface.[11] The creation of defects in the near-surface region of plasma processed semiconductors is well documented.[2,8,11,12] The plasma-processing-induced defects may introduce energy levels in the band gap of the semiconductor that are efficient recombination centers. These centers have an adverse effect on the lifetime of minority carriers, leading to degraded properties of the solar cells.[8,13] Defect creation during plasma processing of semiconductors has been an obstacle for the adoption of dry processing in the fabrication of solar cells and has been the main driving force behind the design and implementation of near-damage-free plasma processing for PV applications.[2–4]

In order to judge the desirability of etching through dielectric layers to the Si substrate, intimate knowledge of the electrical properties of reactive ion etched Si is required. In this study, we have investigated reactive ion etching of both dielectrics and bare Si in CHF_3 plasma with the addition of either O_2 or Ar plasma. For the bare Si samples, deep level transient spectroscopy and minority carrier lifetime measurements are used to characterize the electrical properties of defects introduced in the near-surface region. The surface recombination velocity in etched samples was also determined from the minority carrier lifetimes.

II. EXPERIMENT

RIE was performed in an Oxford PlasmaLab80 system using CHF_3 plasma with the addition of either O_2 or Ar. The process pressure was 55 mTorr and the total gas flow rate was kept constant at 55 SCCM (SCCM denotes cubic centimeter per minute at STP). Samples were placed on the water-cooled (23–24 °C) bottom electrode that was powered by a 13.56 MHz rf generator. The parallel upper and lower electrodes are 240 mm in diameter. In this study, the exposure time, gas flow ratio, or rf power was varied at any one time. The rf powers reported are forward powers, as the measured reflected power was insignificant. Experiments were performed using either O_2 or Ar additives to the CHF_3 plasma. The etch rate of dielectrics were measured on single-sided polished Si wafers that were either oxidized thermally (SiO_2) or had received Si_3N_4 by low-pressure chemical vapor deposition. The thickness of dielectric layer etched for a fixed time was determined using reflectance measurements. The etch rate of Si was determined by etching mesas on patterned surfaces, followed by measurement with an alpha-step stylus profilometer.

For studying RIE-induced defects, we used both *p*- and *n*-type Si wafers from boron- and phosphorus-doped float zone (FZ) ingots. The *p*-type samples had resistivities of 0.75–1.25 Ω cm [(111) orientation] and 140–150 Ω cm [(100) orientation], while the *n*-type FZ wafers had resistivity of 0.8–1.5 Ω cm [(100) orientation]. The wafers were polished in a $HF:HNO_3$ mixture (1:12 by volume) and cleaved into quarters prior to RIE. The samples were between 480 and 500 μm thick. The samples were simultaneously exposed to either a CHF_3/O_2 or CHF_3/Ar plasma for 1 min at rf powers varying between 0 (control) and 250 W. The flow rate of CHF_3 was 50 SCCM and the flow rate of O_2 or Ar was 5 SCCM. After RIE, the samples received standard SC 1 and 2 chemical cleaning procedures that are used in the processing of Si solar cells. The surfaces of these samples were then passivated using plasma-enhanced chemical vapor deposited SiN:H layers deposited at 400 °C.[14] Control samples that did not receive RIE were subjected to identical cleaning and surface passivation steps as the plasma-treated samples. The control samples allow the recombination rate due to all processes other than those caused by RIE, such as recombination at the surfaces, and recombination in the bulk due to Auger recombination and potential contamination arising from the cleaning steps, to be measured. In order to investigate the depth to which the plasma processed surfaces were damaged, samples that were etched at 200 W received post-RIE chemical etching in a mixture of $HF:HNO_3$ (1:12 by volume) for either 1 or 3 min before receiving surface passivation. We chose 200 W for these experiments since this rf power is typically used in the fabrication of our novel thin-film solar cells.[9] We have also investigated the effect of adding a 5 min etch in CARO's solution (3:1 by volume of H_2SO_4 and H_2O_2) between the RIE step and the passivation step on the lifetime of the high-resistivity *p*-Si samples.

The carrier lifetimes were determined using the quasi-steady-state photoconductance method,[15] which measures the lifetime as a function of excess carrier density Δn. Hence, lifetime comparisons between wafers at the same value of Δn can be made, which, depending on the magnitude of the lifetime, may not correspond to the same illumination inten-

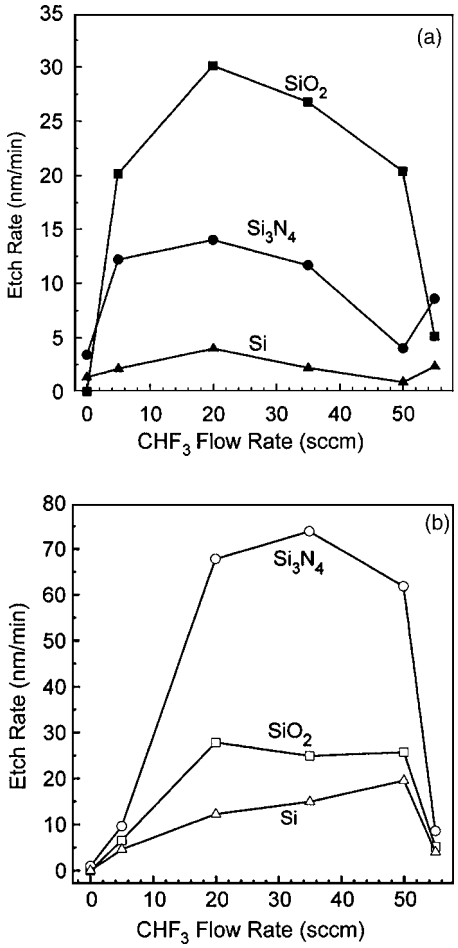

FIG. 1. Etch rates of dielectrics and Si as a function of CHF_3 flow rate in (a) CHF_3/Ar and (b) CHF_3/O_2 plasma. The total gas flow rate, rf power, and process pressure were 55 SCCM, 200 W, and 52 mTorr, respectively, in both cases.

sity. The measured quantity is known as an effective carrier lifetime τ_{eff} and incorporates the impact of recombination both in the bulk and at the surfaces. Deep level transient spectroscopy (DLTS) was performed on the control and plasma-etched 1 Ω cm *p*-FZ and 1 Ω cm *n*-FZ samples using a modified lock-in-type setup.[16] The zero-bias depletion layer width in the low-resistivity samples is ~0.32 μm, which allows the near-surface region of the plasma processed Si to be probed by DLTS. Schottky diodes were fabricated on *p*- and *n*-Si by thermal evaporation of Al/Ti and Au, respectively (~75 nm thick and 0.5 mm diameter) through a metal contact mask. The electrical "signature" of a defect (i.e., energy position in the band gap E_T and apparent capture cross section σ_a) was extracted from a plot of $\ln(T^2/e)$ vs $1000/T$, where e is the emission rate and T is the measurement temperature. This methodology gives only the apparent capture cross section σ_a of the defect, since it is assumed that the defect has a temperature-independent capture cross section.

III. RESULTS AND DISCUSSION

A. Variation of etch rates with gas flow ratio

The variation of Si and dielectric etch rates in CHF_3/Ar is shown in Fig. 1(a) as a function of CHF_3 flow rate. Several

TABLE I. Ratio of SiO_2, Si_3N_4, and etch rates in CHF_3/O_2 to those in CHF_3/Ar as a function of CHF_3 flow rate. The total gas flow, process pressure, and rf power were 55 SCCM, 52 mTorr, and 200 W, respectively.

Material	5 SCCM	20 SCCM	35 SCCM	50 SCCM	55 SCCM
SiO_2	0.5	0.9	0.9	1.4	1
Si_3N_4	0.8	4.9	6.3	15.5	1
Si	2.2	3	6.8	22.8	1

observations can be made from Fig. 1. First, as expected the etch rates in Ar (i.e., 0 SCCM CHF_3) or CHF_3 (i.e., 55 SCCM) only are lowest, showing that the purely physical or chemical etching components of RIE are quite small. RIE is most efficient for a combination of ion bombardment and chemical etching. Second, the etch rate of SiO_2 is highest, followed by Si_3N_4, and then Si. This is consistent with the different abilities of the dielectrics and Si to build up a protective polymer layer on the surface during etching. In CHF_3 plasma, polymer-forming radicals can deposit on the substrate to form a barrier layer consisting of various bonds of carbon and fluorine (i.e., CF_i, $i=1,2,3$). This protective layer acts as a diffusion barrier for both F radicals to reach the surface of the material to be etched and also for volatile compounds, such as SiF_4, to diffuse out. Hence, the etch rates of dielectrics and Si are inversely proportional to the thickness of this polymer layer.[17] There are two factors that influence the thickness of the protective polymer, namely, (1) ion-bombardment-induced sputtering and (2) the presence of reactive species that scavenge the polymer layer. A previous study has shown that without dc bias the etch rate will decrease significantly because of the absence of ion bombardment that removes the polymer layer.[18] The influence of ion bombardment on the etch rate of dielectrics and Si will be discussed further in the next section. It has also been shown that SiO_2, Si_3N_4, and Si have different abilities to consume carbon species during etching.[17] Among the three layers, SiO_2 reacts strongest with fluorocarbon followed by Si_3N_4 and Si. This is because oxygen in the oxide layer provides additional reaction channels with carbon in the polymer layer over nitrogen in the nitride layer. Hence, the polymer layer is thickest on Si and thinnest on SiO_2, which is probably the most significant factor producing the differences between the etch rates of the three layers, as shown in Fig. 1(a). The addition of Ar to the plasma does not provide any additional chemical reaction channels for the removal of the polymer layer. Its only effect on the barrier layer is by sputtering, which is similar for all three materials.

For comparison, we have also measured the etch rate of dielectrics and Si in CHF_3 with addition of O_2. The results are shown in Fig. 1(b). Two significant differences can be noted between Figs. 1(a) and 1(b). A pronounced increase in the etch rate of Si_3N_4 can be observed between 10 and 50 SCCM. The enhancement factors are given in Table I. The addition of O_2 in the plasma provides additional reaction paths that decrease the thickness of the polymer barrier layer on Si_3N_4. This result shows that the polymer barrier layer

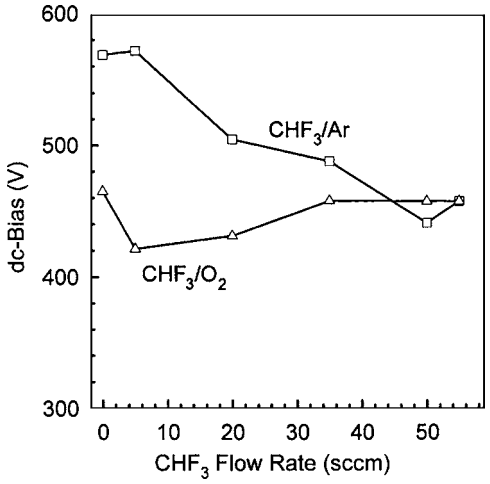

FIG. 2. Variation of dc bias as a function of CHF_3 flow rate for CHF_3/Ar (open squares) and CHF_3/O_2 (open triangles) plasmas.

thickness is larger in CHF_3/Ar plasma than in CHF_3/O_2 plasma. The same can be observed for Si where the enhancement factors are even higher than for Si_3N_4. As expected, the changes in the etch rate of SiO_2 are only marginal. In this case, the oxygen in the oxide layer is already effective at minimizing or suppressing the formation of the barrier layer. Further, the etch rates of especially the dielectrics appear to be fairly constant between 20 and 50 SCCM in Fig. 1(b), compared to their gradual decrease in Fig. 1(a). This difference can be explained by the different self-dc biases generated by CHF_3/Ar and CHF_3/O_2 plasmas, as shown in Fig. 2. The dc self-bias in CHF_3/O_2 is fairly constant (or even slightly increasing) over the CHF_3 range studied here, whereas it is decreasing for CHF_3/Ar plasma. The decrease in the etch rates in CHF_3/Ar with the increasing CHF_3 flow rate up to 50 SCCM may correspond to a decrease in the physical sputtering component of etching.

We have summarized the changes in SiO_2-to-Si_3N_4 etch selectivity in the two plasmas in Table II. The results clearly show that the etch selectivity between SiO_2 and Si_3N_4 can be reversed by substituting O_2 for Ar as an additive to the CHF_3 plasma.

B. rf-power dependence of etch rates

We now turn to the rf-power dependence of the etch rate of dielectrics and Si. Figure 3(a) shows the variation of etch rate for dielectrics and Si as a function of rf power for both

TABLE II. SiO_2-to-Si_3N_4 etch selectivity as a function of CHF_3 flow rate with costant total gas flow rate of 55 SCCM, contstant rf power of 200 W, and constant process pressure of 52 mTorr.

	CHF_3 flow rate (SCCM)					
	0	5	20	35	50	55
CHF_3/Ar	0	1.7	2.1	2.3	5.1	0.6
CHF_3/O_2	0	0.7	0.4	0.3	0.4	0.6

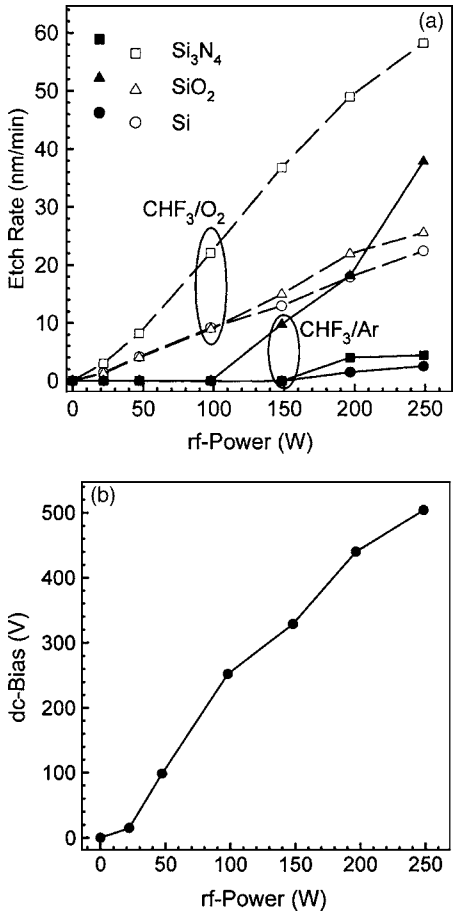

FIG. 3. (a) rf-power dependence of the etch rates of Si_3N_4 (squares), SiO_2 (triangles), and Si (circles) in CHF_3/Ar (solid symbols) and CHF_3/O_2 (open symbols), and (b) variation of dc bias against rf power. Similar rf-power dependencies were observed for both plasmas. The flow rate of CHF_3 was 50 SCCM and that of Ar or O_2 was 5 SCCM, while the process pressure was 52 mTorr.

CHF_3/Ar (solid symbols) and CHF_3/O_2 (open symbols). The gas flows were 50 SCCM CHF_3 and 5 SCCM Ar or O_2. The data points for CHF_3/O_2 reactive ion etching are taken from our previous study and are included here for comparison only.[19] In general, the increase in etch rate with rf power is due to the increase in the physical component of etching (i.e., sputtering), as shown by the increase in dc bias with rf power in Fig. 3(b). We have measured a similar rf-power dependence of dc bias for both CHF_3/Ar and CHF_3/O_2 plasmas.

In addition to increasing bombardment damage of the exposed surface, we may anticipate the thickness of the protective polymer layer to decrease with the increasing dc bias. In fact, a previous study of RIE of Si in $CF_4/40\%$ H_2 has shown that there were three regimes for the rf-power dependence of the polymer layer thickness on Si.[20] First, there was an increase in the thickness of the polymer layer (i.e., film deposition) for rf powers below 100 W, followed by a plateau in the thickness between 100 and 200 W. For rf powers above 200 W, there was a dramatic decrease in the polymer layer thickness by approximately one order of magnitude.

The increase in etch rate of dielectrics and Si with decreasing polymer layer thickness is well established.[17,20,21]

Figure 3(a) reveals a significant difference in etch behavior between the two plasmas. Since O_2 effectively minimizes the thickness of the polymer layer as discussed previously, we have explained the monotonic increase in etch rates in CHF_3/O_2 by increasing physical sputtering.[19] In contrast to etching in CHF_3/O_2, there is a threshold rf power for etching to take place in CHF_3/Ar. This result is similar to RIE in CF_4/H_2 observed in Ref. 20, where etching of Si was observed only at the highest rf powers—a result concomitant with the sudden decrease in the fluoropolymer layer thickness observed in RIE experiments.[20] Since the thickness of this polymer layer is thicker on Si_3N_4 than on SiO_2,[17] the threshold for etching Si_3N_4 in CHF_3/Ar is at a correspondingly higher rf power (i.e., higher dc bias). A thickest barrier layer on Si implies that its etch rate is the lowest in CHF_3/Ar.[17]

C. Effective carrier lifetime in Si

It is of practical importance in the fabrication of solar cells to investigate the interaction of the plasma with the Si substrate when no intervening dilelectric layer is present. As mentioned earlier, the processing steps in the fabrication of our novel micromachined thin-film solar cells can be reduced,[9] implying less wet chemical processes, if dielectric layers can be overetched (i.e., exposing the Si substrate to RIE). The minority carrier lifetime is the electronic property of importance for solar cells. We have, therefore, investigated the rf-power dependence of effective carrier lifetime in both high- and low-resistivity FZ Si.

Based on the Shockley-Read-Hall (SRH) theory of carrier generation and recombination at a discrete defect level with energy, E_T, the SRH lifetime can be expressed as[22,23]

$$\tau_{\mathrm{SRH}} = \frac{\tau_{n0}(p_0 + p_1 + \Delta n) + \tau_{p0}(n_0 + n_1 + \Delta n)}{(p_0 + n_0 + \Delta n)}, \tag{1}$$

where $\Delta n = \Delta p$ is the excess carrier density. The capture time constants τ_{n0} and τ_{p0} are related to the thermal velocity (ν_{th}), the recombination center density (N_t), and capture cross section (σ) via $\tau_{n0} = 1/(\nu_{\mathrm{th}}\sigma_n N_t)$ and $\tau_{p0} = 1/(\nu_{\mathrm{th}}\sigma_p N_t)$. It becomes clear from Eq. (1) that $1/\tau_{\mathrm{SRH}}$ is proportional to the density of the recombination center, N_t. The change in defect concentration, ΔN_t, due to RIE at different rf powers relative to the control sample is proportional to the inverse of lifetime arising from RIE-induced defects, i.e., τ_{defect}. This relationship is expressed as

$$\frac{1}{\tau_{\mathrm{defect}}} = \frac{1}{\tau_{\mathrm{rf\ power}}} - \frac{1}{\tau_{\mathrm{control}}} \propto \Delta N_t, \tag{2}$$

where $1/\tau_{\mathrm{rf\ power}}$ is the inverse lifetime measured at a given rf power and $1/\tau_{\mathrm{control}}$ corresponds to the inverse lifetime of the reference sample. Figure 4(a) shows the variation of $1/\tau_{\mathrm{defect}}$ with rf power for various resistivities and types of Si substrates, as well as plasma mixture. Measurements of

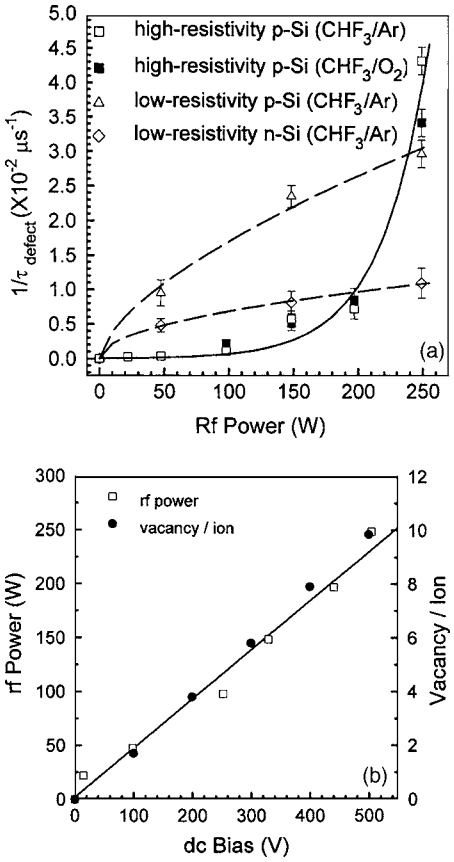

FIG. 4. (a) Variation of RIE-defect-related carrier lifetime with rf power in CHF_3/Ar (open squares) or CHF_3/O_2 (solid squares). Samples were of 150 Ω cm *p*-type Fz Si and exposed to the plasma for 1 min. The gas flow rates were CHF_3=50 SCCM and Ar/O_2=5 SCCM, and the process pressure was 52 mTorr. The solid line is a least-squares fit to data points. The data points shown in open triangles and open diamonds correspond to low-resistivity (1 Ω cm) *p*- and *n*-type Si samples, respectively, etched in CHF_3/Ar plasma. The dashed lines through the data points describe power law relationships. (b) The linear variation of rf power (solid circles) and vacancy production (open squares) with dc self-bias.

$\tau_{\mathrm{rf\ power}}$ and τ_{control} were made at an excess carrier concentration of $\Delta n = 1 \times 10^{15}$ cm^{-3}.

The data points obtained from high-resistivity *p*-Si exposed to CHF_3/Ar or CHF_3/O_2 are shown in the open and solid squares, respectively. These data points overlap reasonably well, suggesting that the type and extent of damage created by the two plasmas in the high-resistivity samples may be quite similar. The solid curve is an exponential fit to all the data points (i.e., both plasmas) measured from the high-resistivity *p*-Si samples [$1/\tau_{\mathrm{defect}} \alpha \exp(0.027 \times \mathrm{rf\ power})$]. We have also performed measurements on low-resistivity *n*- (open diamonds) and *p*-type (open triangles) Si exposed to CHF_3/Ar at different rf powers. In contrast to the results on high-resistivity samples, the rf-power dependence on low-resistivity samples followed a power law [i.e., $1/\tau_{\mathrm{defect}} \alpha$ (rf power)$^{0.50}$ for *n*-type Si, and $1/\tau_{\mathrm{defect}} \alpha$ (rf power)$^{0.64}$ for *p*-type Si].

These rf-power dependencies are quite counterintuitive since one may expect the damage created from RIE to scale up linearly with rf power. For example, we have used TRIM

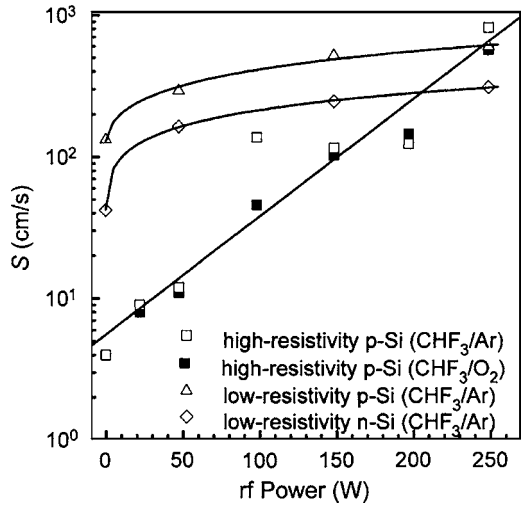

FIG. 5. Surface recombination velocities as a function of rf power.

simulations to calculate the number of vacancies that are produced from CHF_2^+ ion bombardment of Si at energies corresponding to the dc bias generated by CHF_3/Ar or O_2. The results shown in Fig. 4(b) demonstrate that there is indeed a linear correlation between the generation of primary defects and rf power (or dc bias). If lifetime degradation in reactive ion etched samples were due to primary defects, such as vacancies or interstitials, then, from the linearity of the SRH equation in N_T, we would expect that $1/\tau_{\text{defect}}$ would vary linearly with the rf power. However, the rf-power dependence of $1/\tau_{\text{defect}}$ shown in Fig. 4(a) is clearly nonlinear, implying that the RIE-induced lifetime degradation in the FZ Si was not dominated by the production of primary defects. It is possible that the recombination centers responsible for the lifetime degradation arise from complex defect reactions involving primary defects and impurities either during the RIE process or the deposition of SiN_x:H layers at 400 °C. The results shown in Fig. 4(a) further suggest that these defect reactions may be dependent on the doping level of the samples. Since it is not possible to measure lifetimes on unpassivated Si samples, we cannot distinguish between the recombination effect of defects created during RIE and those that may be created during nitride deposition. We will demonstrate that there are indeed defect transformations that take place in our samples during the nitride deposition step at 400 °C when we discuss DLTS results in Sec. III F.

D. Surface recombination velocity

The surface of a semiconductor is the region of highest disturbance due to termination of the long-range order of the lattice. The surface recombination velocity S describes the tendency of the surface to bring down an excess carrier concentration to its equilibrium state. A high value of surface recombination velocity describes a bad state of the surface as excess carriers recombine very fast. The effectiveness of a surface passivation scheme can therefore be gauged by a measure of S. Furthermore, processing of the surface with energetic particles will alter S. The excess carrier lifetime

TABLE III. Recovery of effective carrier lifetime in high-resistivity p-Si after post-RIE Si etching. Samples were exposed to 200 W CHF_3/Ar or CHF_3/O_2 for 1 min.

Post-RIE etch time (min)	Excess carrier lifetime (μs) CHF_3/O_2	Excess carrier lifetime (μs) CHF_3/Ar
0	115	134
1	1800	3300
3	5700	5600

that is measured from photoconductance measurements can be used to determine S. It has been shown that for excess carrier lifetimes exceeding 20 μs, the simple equation (3) can be used to determine S,[24]

$$\frac{1}{\tau_{\text{rf power}}} = \frac{1}{\tau_b} + \frac{2S}{W}. \tag{3}$$

In Eq. (3), τ_b is the bulk lifetime and W is the thickness of the sample. Further assumptions have to be made regarding τ_b before S can be calculated. For FZ crystalline Si (i.e., a high quality crystal lattice that has virtually no recombination centers), it can be assumed that the bulk lifetime is equal to the Auger lifetime τ_{Auger}. If, in reality, the bulk lifetime is lower than the Auger lifetime, the S values determined are then *upper bounds* on S. The Auger lifetime has been determined using a general parametrization which is valid for both low- and high-injection levels.[25] Using this procedure, we have determined the Auger lifetime, and hence bulk lifetime, to be 242 ms in the high-resistivity p-Si, and 2.7 and 5.3 ms in the low-resistivity p- and n-type Si, respectively. The variation of S as a function of rf power for high- and low-resistivity samples is shown in Fig. 5, and as expected they show similar rf-power dependencies as in Fig. 4(a). In high-resistivity p-Si, RIE degraded the quality of the surface by two orders of magnitude over the rf-power range studied here. The difference between the surface recombination velocities measured from low-resistivity p- and n-type Si can be attributed to their different crystallographic orientations. The passivation of $\langle 111 \rangle$ surfaces is generally poorer than that of $\langle 100 \rangle$ surfaces because of the higher density of surface states on the former surfaces by a factor of 3.[26]

E. Post-RIE chemical processing

We now turn to the influence of two post-RIE chemical treatments on lifetime of reactive ion etched samples. In the first experiment, samples that had been exposed to CHF_3/Ar or CHF_3/O_2 for 1 min were etched in a mixture of $HF:HNO_3$ solution for either 1 or 3 min. The results of this experiment are given in Table III. After etching for 3 min, the excess carrier lifetimes in the plasma-treated samples had recovered to their values in the control samples. We have estimated that the amount of Si etched by this chemical treatment in 3 min to be $\sim 10-15$ μm. These are useful information for practical device processing but need further qualification. Typically, practical devices contain doped surface

TABLE IV. Effect of CARO's etch on lifetime recovery in high-resistivity *p*-Si that had been exposed to a CHF_3/Ar plasma at 200 W for 1 min.

	Excess carrier lifetime (μs) CHF_3/O_2	Excess carrier lifetime (μs) CHF_3/Ar
Without CARO's etch	115	134
With CARO's etch	349	349

layers that make up the diode junction and/or a backsurface field, and for metallization. Post-RIE chemical etching to recover the bulk lifetime will also remove any prediffused layers (i.e., doped layers) that typically extend less than 1 μm below the surface (at least for solar cells). Hence, the application of the combination of RIE and a post-RIE Si etch will have to be used in situations where either the surface exposed to the plasma is not doped or when the diffusions can be done after the RIE step. It is also worth noting that the end of range of plasma particles reaching the surface with energy ~400 eV will be between 2–3 nm below the surface. Etching for 1 min is expected to remove up to 5 μm of Si. The partial recovery of the lifetime reveals that some of the defects responsible for lifetime degradation in plasma processed samples already diffuse over ~5 μm during RIE at 23 °C.

A post-RIE treatment in CARO's solution recovered the excess carrier lifetime partially. As shown by the data summarized in Table IV, the lifetime of plasma processed samples that received CARO's etching increased by a factor ~3. A likely explanation for this lifetime recovery is as follows. It is well established that solutions containing H_2O_2 can form chemical oxides on the surface of Si.[27,28] These studies have focused mainly on solutions containing a mixture of H_2O_2 and NH_3. In this solution, the competing processes of oxidation of the Si surface and dissolution of the oxide layer take place.[27] Indeed, a previous experiment using H_2O_2–NH_3 mixture has shown that up to 1 nm of passivating oxide may grown on a Si surface.[27] Since the H_2O_2:H_2SO_4 mixture used here is a very strong oxidizing agent we propose that the buildup of an oxide layer on the surface of the Si surfaces consumes at least part of the damaged layer. This oxide layer is removed using a dilute HF dip prior to deposition of the SiN_x:H passivation layer. Since the end-of-range damage is confined within the top 2–3 nm of the surface, the thickness of the chemical oxide does not have to be particularly thick to produce the lifetime recovery depicted in Table IV.

F. Deep level transient spectroscopy

In order to obtain more information on the electrical properties of defects in plasma-etched Si, we have performed DLTS measurements on both *n*- and *p*-type samples. For this, we have exposed samples for 1 min at a rf power of 250 W using 50 SCCM CHF_3/5 SCCM Ar. Figure 6(a) shows the DLTS spectra from the *n*-type Si. The control samples (solid squares) contained no deep levels. Following RIE, an electron trap, RIE(E1), is detected in the sample exposed to the plasma. Since samples are heated to 400 °C during deposition of SiN:H, we have subjected a RIE etched sample to the same thermal treatment prior to diode fabrication. The DLTS spectrum from the etched *n*-Si heated to 400 °C is shown in solid triangles in Fig. 6(a). The signature of a defect—i.e., energy position in the band gap, E_T, and apparent capture cross section σ_a—was extracted from Arrhenius-like plots of $\ln(T^2/e)$ vs $1000/T$ (where e is the carrier emission rate and T is the measurement temperature), as shown in Fig. 7. This method gives a thermal activation energy that is uncorrected for any temperature dependence of the capture cross section and hence gives an *apparent* capture cross section. Table V summarizes the "signatures" of the defects observed in reactive ion etched *n*- and *p*-type Si.

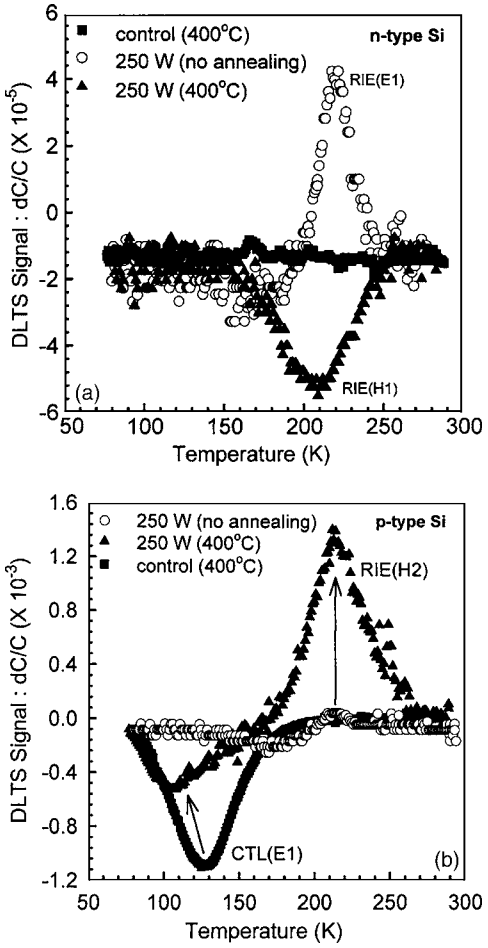

FIG. 6. DLTS spectra measured from low-resistivity (a) *n*-type and (b) *p*-type Si exposed to a 250 W CHF_3/Ar plasma for 1 min. The data points shown as solid squares are from the control sample annealed at 400 °C. The open circles are data points measured on the plasma processed samples, while data points shown in solid triangles correspond the reactive ion etched and annealed samples.

The energy position of RIE(E1) and its capture cross section are $E_T=[E_C-(0.57\pm0.05)\ \text{eV}]$ and $\sigma_a=1.8\times10^{-12}\ \text{cm}^2$, respectively. The signature of RIE(E1) should be treated with caution, since its DLTS peak overlaps with that of a minority carrier trap RIE(H1). The minority carrier defect peak [solid

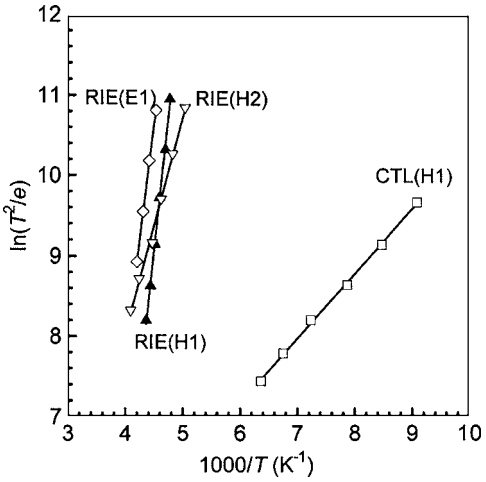

FIG. 7. Arrhenius-like plots of $\ln(T^2/e)$ vs $1000/T$ (where e is the carrier emission rate and T is the measurement temperature) from which the electrical "signatures" of defects were extracted.

triangles in Fig. 6(a)] is prominent in the etched sample annealed at 400 °C. RIE(H1) has an energy position at $[E_V + (0.57 \pm 0.03\ \text{eV})]$ in the band gap and a capture cross section $\sigma_a = 3.9 \times 10^{-14}\ \text{cm}^2$.

We now turn to the DLTS spectra taken from *p*-type Si [see Fig. 6(b)]. The untreated sample (i.e., no RIE and no annealing, not shown in the figure) did not contain electrically active defects that could be detected by DLTS. However, in the control sample, a relatively shallow minority carrier trap CTL(E1) with energy position at $[E_C - (0.09 \pm 0.02)\ \text{eV}]$ and having an unusually small capture cross section of the order of $\sim 10^{-23}\ \text{cm}^2$ (this relates to its relatively less steep Arrhenius plot in Fig. 7) is observed in the control sample after annealing. The unusual signature of CTL(E1) has prompted us to investigate whether it was an artifact arising from the sample structure. It has been shown that the peculiar features such as negative DLTS peaks can be obtained from highly resistive samples.[29] Using the methodology prescribed by Broniatowski *et al.*,[29] we have calculated that an artificial DLTS peak similar to that of CTL(E1) would require a sample series resistance greater than 3121 Ω. We have fitted the forward current-voltage curve (not shown) measured at 114 K on the test structure and found that its series resistance was around two orders of magnitude lower than the threshold resistance required for the appearance of an artificial DLTS peak. Hence, the peak CTL(E1) is most likely to be a defect-related DLTS peak. Since the minority carrier lifetime is quite high in our control samples—i.e., samples that received SiN_x:H passivation at 400 °C—it can be concluded that the presence of CTL(E1) does not affect the carrier lifetime in *p*-type samples. Hence, the creation of CTL(E1) is not of major concern in this study.

What is more important here is the formation of RIE(H2) in the plasma processed and annealed *p*-type sample. The plasma processed sample does not show sign of containing large defect concentrations, albeit that a small defect RIE(H2) peak can be observed [open circles in Fig. 6(b)]. A negative peak around 170 K shows the presence of minority carrier traps in the plasma processed sample. After annealing at 400 °C, the intensity of RIE(H2) increased. Although RIE(H2) superficially appears to be similar to RIE(H1), the two defects have different signatures. The energy position of RIE(H2) is $[E_V + (0.23 \pm 0.03)\ \text{eV}]$ and its capture cross section $\sigma_a \sim 10^{-20}\ \text{cm}^2$. The signature of RIE(H2) is influenced by the presence of the minority carrier defect peak around 110 K. This minority carrier defect peak is most probably due to CTL(E1) with its peak position appearing at a lower temperature due to the overlapping defect peak RIE(H2).

Although it is difficult to further analyze defects RIE(H1) (*n*-type Si) and RIE(H2) (*p*-type Si), two pertinent remarks that are relevant to the present study can be made. First, both are secondary defects that are created during annealing at 400 °C. Regarding samples prepared for minority carrier lifetime measurements, this moderate temperature step is associated with the deposition of the SiN:H surface passivating layer. Hence, the DLTS results shown in Fig. 6 support our earlier suggestion that minority carrier lifetime degradation in plasma processed samples was not due to primary defects created solely by low-energy ion bombardment of samples exposed to the plasma. Second, the intensity of RIE(H2) is larger than that of RIE(H1)—about 40 times from Figs. 6(a) and 6(b). Although the intensities of RIE(H1) and RIE(H2) are not accurate due to the presence of overlapping minority

TABLE V. Summary of electronic properties of defects observed in low-resistivity *n*- and *p*-type Si exposed to 250 W CHF_3/Ar or CHF_3/O_2 for 1 min.

Defect label	Energy position E_T (eV)	Apparent capture cross section σ_a (cm^2)	Remarks
RIE(E1)	$E_C - (0.57 \pm 0.05)$	1.8×10^{-12}	Observed in *n*-Si after RIE. It is annealed out following heat treatment at 400 °C.
RIE(H1)	$E_V + (0.57 \pm 0.03)$	3.9×10^{-14}	Observed in reactive ion etched *n*-type after annealing at 400 °C
CTL(E1)	$E_C - (0.09 \pm 0.02)$	$\sim 10^{-23}$	Observed in unetched *p*-Si annealed at 400 °C
RIE(H2)	$E_V + (0.23 \pm 0.03)$	$\sim 10^{-20}$	Observed in reactive ion etched *p*-type after annealing at 400 °C

carrier traps CTL(E1) and RIE(E1), respectively, we may assume with enough confidence that the peak intensity of RIE(H2) is larger than that of RIE(H1). This result is in qualitative agreement with the lower minority carrier lifetimes measured on *p*-type Si compared to *n*-type Si [data points in open triangles compared to data points in open diamonds in Fig. 4(a)].

IV. CONCLUSION

In summary, we have investigated the use of reactive ion etching of dielectrics and Si in CHF_3/O_2 and CHF_3/Ar plasmas for PV applications. The addition of either O_2 or Ar to CHF_3 can be used effectively to change the etch selectivity between SiO_2 and Si_3N_4, as shown by the rf-power and gas flow rate dependencies. The extent of minority carrier lifetime degradation was observed to be similar in both types of plasmas, showing that the defect reactions leading to a decrease in minority carrier lifetime in samples were similar in both plasmas. In contrast, the lifetime degradations in *n*- and *p*-type Si were different. The lifetime degradation did not exhibit a linear dependence on dc bias (rf power), which suggests that any defects acting as recombination centers were not produced in primary bombardment events. DLTS measurements have shown that indeed secondary defects were formed in samples exposed to the plasma after annealing at 400 °C, which is the temperature at which a silicon nitride layer in deposited on samples to passivate their surfaces. This result has implications for practical devices since one of the last steps in device fabrication is the sintering of metals between 350 and 450 °C for making electrical contacts. We have also shown that post-RIE chemical treatments could be used to reduce the minority carrier lifetime degradation of reactive ion etched samples.

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