

# Damage studies in dry etched textured silicon surfaces

G. Kumaravelu <sup>a</sup>, M.M. Alkaisi <sup>a,\*</sup>, A. Bittar <sup>b</sup>, D. Macdonald <sup>c</sup>, J. Zhao <sup>d</sup>

<sup>a</sup> Department of Electrical and Computer Engineering, University of Canterbury, Private Bag 4800, Christchurch 8020, New Zealand

<sup>b</sup> IRL, Lower Hutt, Wellington, New Zealand

<sup>c</sup> Faculty of Engineering, The Australian National University, Canberra, ACT 0200, Australia

<sup>d</sup> Centre for Photovoltaic Engineering, University of New South Wales, Sydney, NSW 2033, Australia

## Abstract

Surface texturing is a more permanent and effective solution to eliminate reflections compared with antireflection coatings in optical devices. In this study texturing was performed using a reactive ion etching technique, reflectance was measured and the resultant damage on the surfaces was monitored through the minority carrier lifetime measurements. High minority carrier lifetime is an indication of low defect centres and is essential for maximum collection efficiency. It is found that the reflectance of the textured cone structures is less than 0.4% at wavelengths from 500 to 1000 nm and shows a minimum of 0.29% at 1000 nm. while the reflectivity from black silicon is around 1% and from hole structures is around 6.8% in the same wavelength range. The quasi-steady-state photo conductance technique was used to measure the effective carrier lifetimes of the textured samples, showing that chemical wet etch damage removal is effective in improving the lifetime of the sample.

© 2003 Elsevier B.V. All rights reserved.

PACS: 52.77.Bn; 81.05.-t; 81.65.cf

Keywords: Surface texturing; Reactive ion etching; Solar cell; Photoconductance

## 1. Introduction

Surface texturing for enhanced absorption in Si has been historically obtained by creating randomly distributed pyramids [1] using anisotropic etchants, but this preferential etching works only on single crystalline silicon because of its crystallographic orientations. These techniques are not satisfactory for multicrystalline silicon (mc-Si) solar cells because of the random grain orientation. Several attempts have been made to texture polycrystalline and multi crystalline silicon wafers, including laser-structuring [2], mechanical diamond saw cutting [3], porous-Si etching [4] and mask-less RIE etching which results in so-called “Black silicon” [5]. Also by applying an etch mask to the surface and using isotropic etching, structures can be etched in mc-Si for light confinement [6].

However, most of these generally slow techniques may be too costly to ever be used in large-scale production. This paper presents evidence for the formation

of hexagonal structured cone and hole textures using reactive ion etching, which considerably reduce surface reflections despite the introduction of surface damage. The quasi-steady-state photo conductance (QSSPC) technique [7] is used for the effective lifetime measurement before and after wet defect removal etching to determine the level of RIE induced damage present.

## 2. Surface texturing

Surface texturing has been achieved first using photolithography to define the texturing patterns followed by reactive ion etching for pattern transfer process.

### 2.1. Pattern definition

A chrome-on-glass mask (arrays of 3 μm holes in 4 μm pitch, hexagonally arranged) was used as the lithography mask. We employed subtractive (wet etching) technique for making hole type patterns and an additive (lift-off) technique for making cone type patterns.

\* Corresponding author. Tel.: +64-3-364-2867x7272; fax: +64-3-364-276.

E-mail address: [alkaisim@elec.canterbury.ac.nz](mailto:alkaisim@elec.canterbury.ac.nz) (M.M. Alkaisi).

## 2.2. Reactive ion etching processes

An Oxford PlasmaLab80 Reactive Ion Etcher with cryogenic electrode has been employed for this purpose. Details of texturing technique have been published elsewhere [8].

### 2.2.1. Hole structure formation

Hole structures of 3–4  $\mu\text{m}$  diameter were defined by wet etching the metal (NiCr) etch-mask. Then the wafer was subjected to a 30-min RIE etch at a  $\text{SF}_6/\text{O}_2$  flow rate of 90/10 sccm (where sccm denotes cubic centimetres at STP). This sample was over-etched to eliminate the remaining flat surfaces. The final textured surface of hole type structure is shown in Fig. 1.

### 2.2.2. Cone structure formation

A silicon wafer with arrays of 3–4  $\mu\text{m}$  NiCr dots which were transferred using lift off technique was subjected to an RIE treatment similar to that described in (a). The final textured surfaces of column type are shown in Fig. 2. The column structures ended up with cone structure due to intentional over-etching.

### 2.2.3. Black silicon formation

In this process no intentional mask is used. The black silicon texturing is based on local and regenerating oxide

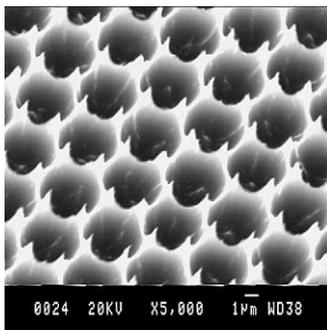


Fig. 1. SEM photograph of hole type texturing. Holes are 7–8  $\mu\text{m}$  deep and in 4  $\mu\text{m}$  pitch.

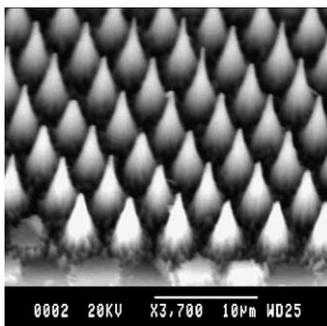


Fig. 2. SEM photograph of cone type structures. Cones are 6–7  $\mu\text{m}$  height and in 4  $\mu\text{m}$  pitch.

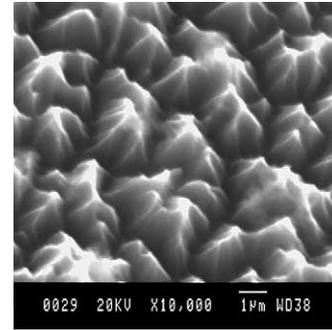


Fig. 3. SEM photograph of black silicon. (No intentional mask is used.)

masking and therefore results in inhomogeneous etching. Initially the surface is covered with native oxide. This masking layer is not removed homogeneously, but perforated first. Unmasked spots are etched and pyramid or needle-like structures are formed depending on the degree of isotropy of the etch process [9] (Fig. 3).

## 3. Reflectance measurement

The diffuse reflectance of the four samples was measured using a purpose-built integrating sphere attachment of a high accuracy spectrophotometer. Fig. 4 shows the measured diffuse reflectance as a function of the wavelength. It can be seen that in all three types of textured surfaces the reflection decreases at wavelengths from 250 to 1000 nm, which include the visible region. The lowest reflection is obtained from the surface of the cone structure and is less than 0.4% at wavelengths from 400 to 1000 nm and shows a minimum of 0.29% which is much less than that of hole structures [8].

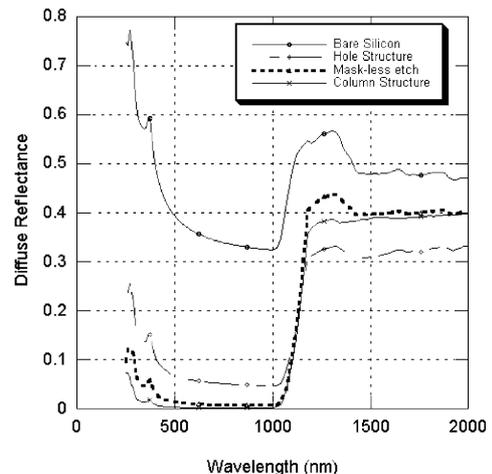


Fig. 4. Diffuse reflection of planar silicon and the textured surfaces of Hole type structure, cone type structure and mask-less etched structure.

#### 4. Effective lifetime measurement

The QSSPC technique was used to measure the effective carrier lifetimes of the textured samples. This technique is based on the simultaneous measurement of the excess conductance of the wafer, through an inductively-coupled coil, and the generation rate, via a calibrated solar cell. Under steady-state conditions, the generation and recombination rates are equal, and the lifetime is simply proportional to the ratio of the excess conductance and the generation rate.

Prior to measurement it is essential to deposit a passivating film; in this case SiN was deposited on the wafer surfaces using PECVD method. In the absence of excessive surface damage, such films reduce surface recombination to the extent that the resulting effective lifetime is often dominated by the bulk lifetime of a sample. This is reflected by the lifetime measurements on the FZ control samples (see Fig. 5), which have planar surfaces produced by chemical etching. It is found that significant surface damage has been introduced after dry etching step and the measured effective lifetime has been reduced accordingly. In the extreme case of an infinite surface recombination velocity, the maximum lifetime measured on the RIE etched silicon wafer was around 2 microseconds when using white light.

After the RIE process, samples were treated by dipping in HNO<sub>3</sub>: HF (50:1) solution for a period of 8 min at room temperature to remove the damaged layer. This step is called defect removal etching (DRE). All effective lifetimes were measured at an excess carrier density of  $1 \times 10^{15} \text{ cm}^{-3}$ . The effective lifetime of the sample after DRE is 36  $\mu\text{s}$ , compared with 2 or 3  $\mu\text{s}$  for the RIE etched sample without DRE. This corresponds to an implied one-sun open-circuit voltage of around 605 mV compared to about 550 mV before DRE. Each order of magnitude increase in lifetime gives an extra 60 mV, since the voltage is logarithmically dependent on the carrier density (and hence lifetime), assuming an ideality

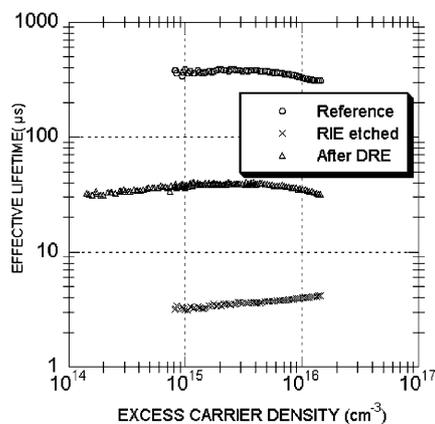


Fig. 5. Excess carrier lifetime of RIE etched Si sample (hole type), after chemical DRE and reference sample.

factor of 1. Thus the damage removal etch can be used to produce low-defect surfaces and further reduction is possible for deeper DRE.

Sub-micron channelling microscopy (QCC) has also been used to study RIE damage on our samples. However, the results of these studies surprisingly show that structural damage is not significant after the dry etching process [10].

#### 5. Conclusion

A reactive ion etching process has been developed for surface texturing. Cone structures, hole structures and mask-less etched structures showed measured reflectance of less than 0.4%, 6.8% and 1.4% respectively at wavelengths from 400 to 1000 nm. This crystal orientation-independent texturing can be used both for monocrystalline and multicrystalline surfaces, but trade off between reflections and RIE induced damage has to be considered and optimised. RIE induced surface damage was evidenced from the QSSPC measurement but it can be removed by stepwise chemical DRE. Optimisation of the size of the textured features and etching process is essential for further removal of the damage.

#### Acknowledgements

The authors would like to acknowledge the contributions from other members of the Nanostructure Engineering Science and Technology Group, Department of Electrical and Computer Engineering, University of Canterbury. This research is supported by the New Economy Research Fund, Foundation for Research, Science and Technology, New Zealand, contract no. UOCX-9905.

#### References

- [1] M.A. Green, *Solar Cells: Operating Principles, Technology and System Applications*, vol. 1, University of New South Wales, Kensington, 1982.
- [2] S. Narayanan, Ph.D. Dissertation, University of New South Wales, Sydney, Australia, 1989.
- [3] P. Path, G. Wileke, E. Bucher, J. Szlufcic, R.M. Murti, K. De Clercq, J. Nijs, R. Mertens, *Proc. 24th IEEE Photovoltaic Specialist Conf.*, 1994, pp. 1347–1350.
- [4] R.R. Bilyalov, L. Stalmans, L. Schirone, et al., *IEEE Trans. Electron Dev.* 46 (1999) 2035–2040.
- [5] H. Jansen, M.D. Boer, R. Legtenberg, et al., *J. Micromech. Microeng.* 5 (1995) 115–120.
- [6] J. Zhao, A. Wang, M.A. Green, et al., *Appl. Phys. Lett.* 73 (1998) 1991–1993.
- [7] R.A. Sinton, A. Cuevas, *Appl. Phys. Lett.* 69 (1996) 2510.
- [8] G. Kumaravelu, M.M. Alkaiasi, A. Bittar, *Proc. 29th IEEE Photovoltaic Specialists Conf.*, 2002, pp. 259–261.
- [9] M. Schnell, R. Ludemann, S. Schaefer, *Proc. 28th IEEE Photovoltaic Specialists Conf.*, 2000, pp. 367–370.
- [10] E.J. Teo, M.M. Alkaiasi, A.A. Bettiol, T. Osipowicz, J. Van Kan, F. Watt, A. Markwitz, *Nucl. Instr. Methods Phys. Res. B* 190 (2002) 339–344.