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Minority carrier lifetime in plasma-textured silicon wafers for solar cells

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Abstract

In this work a comparison between plasma-induced defects by two different SF_6 texturing techniques, reactive ion etching (RIE) and high-density plasma (HDP) is presented. It is found that without any defect-removal etching (DRE), the minority carrier lifetime is the highest for the HDP technique. After DRE, the minority carrier lifetime rises as high as 750 μs for both RIE- and HDP-textured wafers at an excess carrier density of $1 \times 10^{15}\,cm^{-3}$. The measured lifetimes correspond to an implied one-sun open-circuit voltage of around 680 mV compared to about 640 mV before DRE for the HDP-textured wafers. FZ silicon ⟨1 0 0⟩ wafers were used in this study. We also noted that in the RIE process, the induced defect density was significantly lower for wafers etched at 300 K than those etched at 173 K.

Keywords: Reactive ion etching; Surface texturing; Silicon solar cell; Minority carrier lifetime

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1. Introduction

To maximise the efficiency of solar cells, researchers have attempted various solar cell structures aiming to maximise the absorption of incident photons and collection of photogenerated carriers [1,2] One approach is through surface texturing of the silicon wafer to reduce reflections from front surfaces while maintaining high minority carrier lifetime by minimizing process induced defects [3].

Texturing is very effective in reducing reflections and it is especially important for thin films, multicrystalline materials and for capturing long wavelength light. Surface texturing for enhanced absorption in Si has been obtained historically by creating randomly distributed pyramids [4] using anisotropic etchants, but this preferential wet etching works best on single crystalline silicon because of its crystallographic orientations. These wet etching techniques are not satisfactory for multicrystalline silicon (mc-Si) solar cells because of the random grain orientation. Also it places a limitation on the growth of solar production capacity due to the tremendous amount of material, water and chemicals that need to be consumed. Mechanical texturing techniques require wafers with sufficiently thick material for mechanical stability. These methods are not applicable especially for thin, warped and fragile materials. Plasma assisted processing has the potential to be an alternative method for industrial texturing of monocrystalline, multicrystalline and thin film based solar cells.

In this study, texturing was performed using a conventional reactive ion etching (RIE) technique and a high-density plasma (HDP) with electron cyclotron resonance (ECR) source. Reflectance was measured and the resultant damage on the wafer surfaces was monitored through minority carrier lifetime measurements. A high minority carrier lifetime is an indication of low defect concentration and is essential for obtaining high collection efficiency.

The quasi-steady-state photo conductance (QSSPC) technique [5] was used to measure the effective carrier lifetimes of the textured samples, and revealed that chemical wet damage removal etching (DRE) is essential in improving the lifetime of the sample.

We reported previously [6] that reflectance of the textured cone structures by RIE processing was less than 0.4% at wavelengths from 500 to 1000 nm and showed a minimum of 0.29% at 1000 nm. However, the RIE texturing process introduced significant surface defects that resulted in a large drop in carrier lifetime [7].

In this work, we will present a comparison of plasma induced defects caused by two different SF_6 plasma techniques, RIE and HDP with ECR plasma source.

2. Processing techniques

Boron-doped FZ–Si $\langle 1\,0\,0 \rangle$ wafers of base resistivity of 1–10 Ω cm was used in all of this work. RIE texturing was performed using the Oxford Plasmalab 80 RIE system at the Microelectronics laboratory, Department of Electrical and Computer Engineering, Canterbury University, New Zealand. The HDP etching was done at

Delft Institute of Microelectronics and Submicron Technology (DIMES), The Delft University of Technology, Netherlands. For HDP, an ECR plasma source was used. As SF_6/O_2 gas mixtures are more reactive than SF_6, and introduces more defects to the wafer, we concentrated only on SF_6 plasma texturing in this study. In addition, contamination effects on minority carrier lifetime due to oxygen will be isolated from damage induced due to etching. The QSSPC technique was used to measure the effective carrier lifetimes of the textured samples at the Department of Engineering, FEIT, Australian National University, Australia.

2.1. Plasma etching conditions

The processing flow diagram for texturing and wafer preparation for performing minority carrier lifetime measurements is shown in Fig. 1. Minority carrier lifetimes were measured before and after damage-removal etching. Details of wafer preparation and etching is published elsewhere [6].

Fig. 2a shows a scanning electron microscopy (SEM) image for a wafer textured using the RIE technique in SF_6 plasma. In Fig. 2b, texturing is performed using a HDP in SF_6. In both structures the etched depth in silicon was 6–7 μm, but the textured structures obtained are not the same due to different etching mechanisms and rates for RIE and HDP.

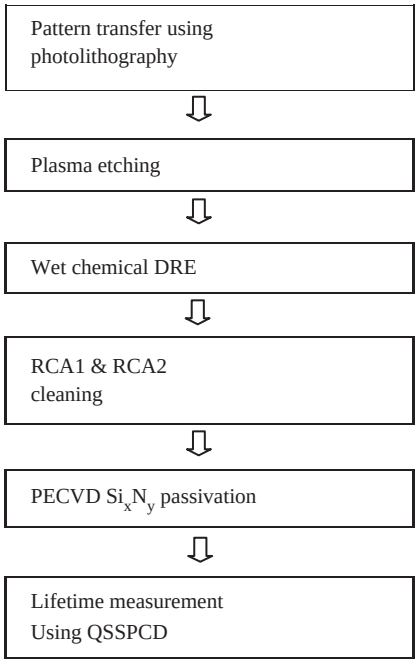

Fig. 1. Schematic of the processes and characterisation involved in plasma-textured silicon wafers.

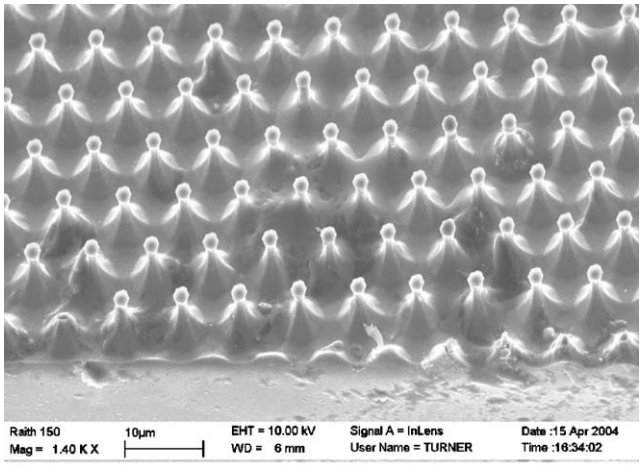

Fig. 2. (a) SEM image of RIE-textured wafer; (b) SEM image of HDP-textured wafer.

A mask with hexagonally arranged circular dots of 8 μm diameter on a ten micron pitch was photolithographically transferred to the silicon wafers and was used as an etch mask for both RIE and HDP processes. AZ 4620 positive photoresist was used as an etch mask in place of the metal etch masks which were used in our previous work. This is to eliminate any lift off processes and develop a method where only dry etching is employed.

2.1.1. RIE parameters

Texturing was performed using RIE in SF_6 gas at 295 K and an RF power of 200 W at 13.56 MHz. The self-biased DC voltage was −105 V. The etching pressure

was maintained at 150 mT and SF_6 flow rate at 160 sccm for all experiments. The resultant etch rate is 1.2 μm min^{-1}. As the Plasmalab80Plus has a cryogenic electrode, we etched one set of wafers at 173 K for a temperature dependence study.

2.1.2. HDP parameters

The wafers were etched for 8 min in the HDP with the ECR source etcher to obtain the 7 μm deep structure.

The microwave power was 400 W set at 2.45 GHz, and a −18 V DC biased was applied. SF_6 flow rate was 22.5 sccm and etching temperature was 250 K. The etching pressure was maintained at 1.5 mT. The etch rate for the HDP was 0.9 μm min^{-1}.

In this study, it should be noted that the main objective is to compare the damage induced in each technique and its effects on the minority carrier lifetime and not to optimise the structure for minimum reflections.

2.2. Defect removal etching (DRE)

Two identical wafers (A, B) were textured using RIE and another two identical wafers (C, D) were textured using HDP. After the plasma etching process, samples B and D were treated by dipping in HNO_3:HF (50:1) solution for a period of 5 min at room temperature to remove the damaged layer which is estimated to be in the order of 2–3 μm. This step is called DRE. The other two wafers (A and C) were not subjected to DRE and used as controls.

3. Minority carrier lifelime measurement

The QSSPC technique was used to measure the effective carrier lifetimes of the textured samples. This technique is based on the simultaneous measurement of the excess conductance of the wafer, through an inductively coupled coil, and the generation rate, via a calibrated solar cell. Under steady-state conditions, the generation and recombination rates are equal, and the lifetime is simply proportional to the ratio of the excess conductance and the generation rate.

Prior to measurement the samples were subjected to a standard RCA1 and RCA2 cleaning, and a SiN surface-passivating film was deposited on the wafer surfaces using a PECVD reactor at the ANU. In the absence of excessive surface damage, such films reduce surface recombination to the extent that the resulting effective lifetime is often dominated by the bulk lifetime of a sample. This is reflected by the lifetime measurements on the FZ untextured wafers (see Fig. 3a top curve) which have flat polished surface produced by chemical etching to remove any surface defects.

It is demonstrated that the plasma-induced damage is very high in the case of RIE-textured wafers compared to the HDP-textured wafers. This is illustrated by the extremely low minority carrier lifetime of less than 10 μS for RIE-treated wafers. However, after the 5 min defect removal etch, the minority carrier lifetime rises as high as 750 μs at an excess carrier density of 1×10^{15} cm^{-3}, as illustrated in Fig. 3a

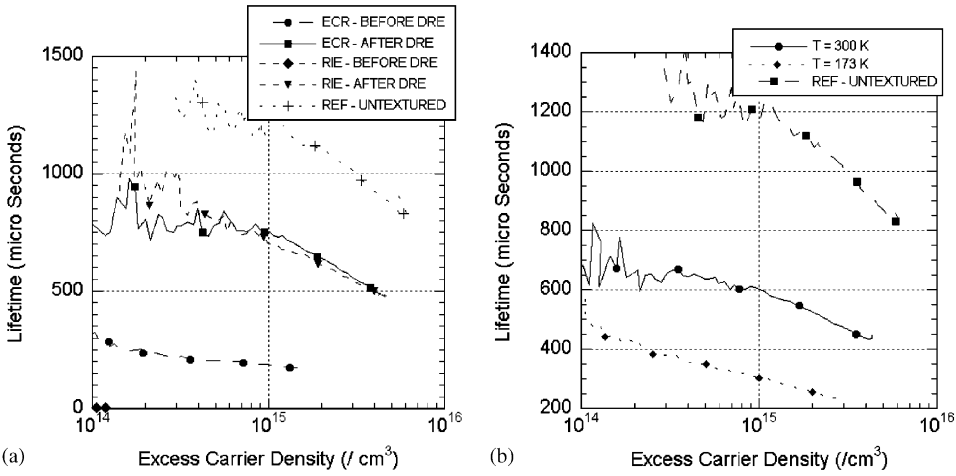

Fig. 3. (a) A comparison of lifetimes of ECR-and RIE-etched Si wafers; (b) Dependence of lifetime on etch temperature.

middle curves. In the HDP-textured wafers, the minority carrier lifetime obtained after the DRE corresponds to an implied one-sun open-circuit voltage of around 680 mV compared to about 640 mV before DRE. It is interesting to notice that for both HDP- and RIE-textured wafers, the minority carrier lifetime can be recovered to such high level after the DRE step.

These results indicate that most of the RIE generated damage propagates into a shallow layer beneath the surface, as it only requires the removal of between 2 and 3 μm to notice a significant improvement in minority carrier lifetime.

It is encouraging to notice that for HDP-textured wafer, the minority carrier lifetime is around 250 μs even before the DRE process which indicates that high open-circuit voltages can be obtained using these textured wafers even without DRE. This illustrates that with the proper choice of plasma conditions an effective plasma texturing process can be achieved.

To study the effects of etching temperature on induced damage for RIE-textured wafers, the minority carrier lifetimes have been measured for wafers etched at 300 K and at 173 K in an SF_6 plasma. It is found that the minority carrier lifetime is significantly higher for wafers etched at 300 K than those etched at 173 K as shown in Fig. 3b. This result is obtained after a 1 min DRE step and indicates that increasing the temperature during etching helps in annealing the structural damage as it forms.

4. Reflectance measurements

The diffuse reflectance of wafers etched using RIE and HDP before and after the DRE step is shown in Fig. 4. Reflectance has been reduced from the 35% for an untextured wafer to around 6% for textured wafers. It is noted that after the DRE

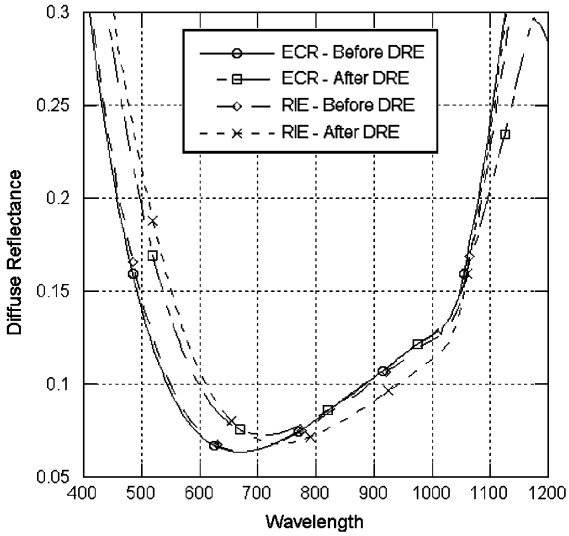

Fig. 4. Diffuse reflectance of HDP-and RIE-etched wafers.

process, the minimum in reflectance is shifted from 650 to 750 nm and that the surface becomes more reflective at the shorter wavelengths. It should be emphasised that for these wafers the prime objective is to compare damage induced in two plasma-etching systems (RIE and HDP) and its effects on minority carrier lifetimes and wafers were not optimised for reflections. To minimise reflections further, denser textured patterns would have to be used. This was demonstrated in our previous publications where less than 0.4% reflectance was achieved [6].

5. Conclusions

Texturing is employed to reduce optical losses on the front surface of silicon wafers.

Surface texturing of silicon wafers is performed by two plasma-etching methods, RIE and high density ECR plasma, to study the effects of the plasma parameters on the damage induced during dry etching processes. Minority carrier lifetime measurements are very sensitive to both structural damage introduced by different etching mechanisms and electronic defects caused by process contamination.

Minority carrier lifetime measurements were performed on textured wafers and found that the RIE-treated wafers have a much lower minority carrier lifetime compared to those etched using HDP. However, in both RIE-and HDP-textured wafers, the minority carriers lifetimes recovered to reach a level of 750 μs after the defect removal step, which is suitable for solar cell applications.

In the HDP etching process, ions have less bombarding energy compared to those that exist in the RIE process. This could be the reason for the lower defect densities

observed in HDP-textured wafers as indicated by the higher minority carrier lifetimes.

In addition, in the HDP process the etching pressure required is lower than that for the RIE and the DC bias was only −18 V, much lower than that for RIE (which was self biased at 105 V). These factors may lead to less damaged wafers in the former process [8].

From our temperature dependence study it is also noted that higher temperature etching produced wafers with less damage, indicating that physical damage is responsible for the observed minority carriers lifetime rather than contamination.

Sub-micron channelling microscopy has also been used to study RIE damage on similarly treated samples. However, the results of these studies surprisingly show that structural damage is not significant after the dry etching process [9], at least to the extent observable with this technique.

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