

Research

Reactive Ion Etching of Dielectrics and Silicon for Photovoltaic Applications

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This paper investigates the reactive ion etching of SiO₂, Si₃N₄, and Si using CHF₃/O₂ plasma. In particular, we have characterized the time and rf power dependence of the carrier lifetimes in n- and p-type FZ Si. The time dependence of reactive ion etching (RIE) at different rf powers provide insight into the two competing processes of damage accumulation and damage removal in the near-surface region of the Si during plasma etching. The carrier lifetime, measured using the quasi-steady-state photoconductance (QSSPC) technique, has a quadratic dependence on the rf power, which can be related to changes in the dc self-bias generated by the plasma at different rf powers. The change in carrier lifetime is similar in both n- and p-type Si of the same doping concentration. Using this fact, together with the electronic properties of defects obtained by deep level transient spectroscopy (DLTS), we have modeled the injection-dependence of the measured carrier lifetimes using the Shockley–Read–Hall model. The isochronal annealing behavior of plasma etched Si has also been studied. Copyright © 2006 John Wiley & Sons, Ltd.

KEY WORDS: reactive ion etching; defects; silicon; dielectrics

INTRODUCTION

Plasma (or dry) etching has become a dominant technique in semiconductor processing because it provides highly anisotropic etch profiles with good selectivity.^{1,2} Although plasma etching is not widely used in the fabrication of solar cells, it has nevertheless found some niche applications. The fabrication of silicon solar cells is still heavily reliant on wet chemical etching and substitution of some or all of these wet chemical steps by dry processing would provide advantages of reduced environmental impact and better safety in the workplace. An earlier study investigating replacement of all wet chemical steps by plasma etching used a combination of SF₆ and CHF₃ plasma etching in an electron-cyclotron-resonance (ECR) plasma reactor.³ The study of Schaefer and Lüdeman demonstrated a nearly damage-free reactive ion etching (RIE) process for solar

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cell processing, whereby dry processed solar cells showed the same performance as wet-etched cells.³ The same group had previously fabricated solar cells with efficiencies up to 17% using a combination of ECR plasma processing and wet chemistry, the latter used only for metallization.⁴ More recently, Gazuz and co-workers have shown the feasibility of large area silicon solar cell processing using plasma etching, and reported a power conversion efficiency of 14.7% for the completely dry-processed cells compared to 15.1% for the wet-processed reference cell.⁵ There have been other specific applications of plasma etching in the fabrication of solar cells, including the formation of buried base contacts,⁶ etching of phosphorous silicate glass,^{4,5,7} and texturing.^{8–10}

RIE proceeds via a combination of physical sputtering and gasification of the exposed semiconductor surface. Hence, RIE of semiconductor surfaces involves two competing processes, namely (1) damage creation in the near-surface region of the surface exposed to low-energy ions, and (2) removal of the damaged layer during etching. The modification of the semiconductor surface by bombarding ions can significantly increase the rate of gas–solid interaction, and hence the etch rate of the semiconductor. However, bombardment of the semiconductor causes lattice damage to build up below its surface, and the cumulative damage during etching depends critically on the relative rates of damage creation and etching of the damaged surface.^{11,12} The creation of defects in the near-surface region of plasma processed semiconductors is well documented.^{3,10–14} In the presence of electrically active defects that may act as recombination centers, the electrical properties of the solar cells usually degrade.^{10,15} Defect creation during plasma processing of semiconductors has been an obstacle for the adoption of dry processing in the fabrication of solar cells, and, as such, is the main driving force behind the design and implementation of near-damage-free plasma processing for photovoltaic applications.^{3–5}

RIE is used in conjunction with wet chemistry in the fabrication of the novel thin-film silicon solar cell developed at the Australian National University.¹⁶ The innovative features of the new cells include the improved Si utilization by a factor ~ 12 ; a reduction in the number of wafers per kW by ~ 30 ; high efficiency and perfect bifacial response. RIE is a versatile and practical option that can be used in the micromachining and metallization steps of this new thin-Si film solar cell technology. Patterning of the silicon surface for micromachining requires detailed knowledge about the etch selectivity between dielectric layers (SiO_2 and Si_3N_4) and Si. Since in some instances it would be highly desirable to over-etch the dielectric layers (i.e. etching to or into the Si surface), the influence of defects generated by exposing the Si to the energetic particles from the plasma on the electrical properties of the substrate must be known. Etching dielectric layers through to the substrate is desirable for several reasons, including reduced device fabrication complexity and minimizing the use of toxic hydrofluoric acid. In this study, we report on the etch rates of SiO_2 , Si_3N_4 , and Si in a CHF_3/O_2 plasma, and on the carrier lifetime of reactive-ion-etched float zone Si. Furthermore, we demonstrate that deep level transient spectroscopy (DLTS) and lifetime measurements are a powerful combination for characterizing the electrical properties of defects for PV applications.

EXPERIMENTAL

RIE was done in a Oxford PlasmaLab80 system using CHF_3/O_2 plasma. The process pressure was 55 mT and gas flow rates were 50 sccm and 5 sccm for CHF_3 and O_2 , respectively. Samples were placed on the water-cooled (23°C) bottom electrode that was powered by a 13.56 MHz rf generator. In our experiments, only the exposure time or rf power was varied.

For measuring the etch rate of dielectrics, we have used single-sided polished Si wafers that were either oxidized thermally (SiO_2) or which received Si_3N_4 by low-pressure chemical vapor deposition (LPCVD). The thickness of dielectric layer etched for a fixed time was determined from the difference between its thickness before and after RIE using reflectance measurements. The etch rate of Si was determined by etching mesas on patterned surfaces. The depth of mesas was measured using an alpha-step stylus profilometer. Etch rate of dielectrics and Si were measured for rf powers up to 250 W.

For studying RIE-induced defects, we used both p- and n-type Si wafers from 4 inch boron- and phosphorus-doped float zone (FZ) ingots. The p-type samples had resistivities of 0.75–1.25 $\Omega\text{ cm}$ and 140–150 $\Omega\text{ cm}$, while the n-type FZ wafers had resistivities of 0.8–1.5 $\Omega\text{ cm}$ and $>100\text{ }\Omega\text{ cm}$. The wafers were polished in a $\text{HF}:\text{HNO}_3$ mixture (1:12 by volume) and cleaved into quarters prior to RIE. The samples were between 480 and 500 μm

thick. In one experiment, 150 Ω cm p-FZ samples were exposed to the plasma for 15 s to 25 min using either 50 or 200 W rf power. We typically use 200 W etching of dielectrics in the fabrication of our novel thin-film Si solar cells.¹⁶ In a second experiment, 150 Ω cm p-FZ and 100 Ω cm n-FZ samples were exposed simultaneously to the plasma for 30 s but at different rf powers. Additionally, 1 Ω cm p-FZ and 100 Ω cm n-FZ samples were exposed at 200 W for either 30 s or 5 min. After RIE, the samples were chemically cleaned prior to light phosphorous diffusion and oxidation. This high temperature step serves two purposes, namely (1) it mimics the post-RIE high temperature processing in our solar cell fabrication scheme, and (2) provides surface passivation for minority carrier lifetime measurements. The surface passivation of samples was completed with a forming gas anneal at 400°C.¹⁷ Control samples that did not receive RIE were subject to identical etching, cleaning, and surface passivation steps as the plasma-treated samples. The control samples allow the recombination rate due to all processes other than those caused by RIE, such as recombination at the surfaces, and recombination in the bulk due to Auger recombination and potential contamination arising from the annealing, etching and cleaning steps, to be measured. In order to investigate the effect of post-RIE isochronal annealing on the minority carrier lifetime, 1 Ω cm p-FZ and 150 Ω cm p-FZ samples that had been subject to 200 W RIE were annealed at 400, 750, or 1050°C in nitrogen. These samples were passivated using plasma-enhanced chemical vapor deposited SiN:H layers,¹⁸ since phosphorus diffusion passivation is not feasible for all of these temperatures.

The carrier lifetimes were determined using the quasi-steady-state photoconductance method (QSSPC),¹⁹ which measures the lifetime as a function of excess carrier density Δn . Hence, lifetime comparisons between wafers at the same value of Δn can be made, which, depending on the magnitude of the lifetime, may not correspond to the same illumination intensity. The measured quantity is known as effective lifetime, τ_{eff} , and incorporates the impact of recombination both in the bulk and at the surfaces. DLTS was performed on the control and plasma-etched 1 Ω cm p-FZ and 1 Ω cm n-FZ samples using a modified lock-in-type setup. We chose these samples for DLTS measurements because of their lower resistivity. In this case, the lower zero-bias depletion layer was small (~ 0.32 μm compared to ~ 3.5 μm for 150 Ω cm material), allowing us to probe defects close to the surface where they are produced during RIE. Prior to diode metallization, the phosphorous-diffused layer of the samples was chemically etched. Schottky diodes were fabricated on p- and n-Si by thermal evaporation of Ti and Au, respectively (~ 75 nm thick and 0.5 mm diameter) through a metal contact mask. The electrical 'signature' of a defect (i.e., energy position in the band gap, E_{T} , and capture cross-section, σ) was extracted from a plot of $\ln(T^2/e)$ versus $1000/T$, where e is the emission rate and T is the measurement temperature. This methodology gives only the apparent capture cross-section, σ_{a} , of the defect, and it is assumed that the defect has a temperature-independent capture cross section.

ETCH RATE OF DIELECTRICS AND SILICON

Figure 1a shows the variation of etch rate of SiO₂, Si₃N₄, and Si as a function of rf power, while Figure 1b shows the power-dependence of etch selectivity (measured as the ratio of etch rates in Figure 1b). Several studies have previously measured the etch rates of Si and dielectrics in CF-based plasmas and several pertinent observations have been made.^{20–25} Etching in CHF₃ plasma usually provides very high selectivity between Si and SiO₂ (or Si₃N₄) because of the formation of a thin polymer layer on Si. This layer limits the rate at which fluorine radicals from the plasma reach the Si surface, as well as the rate of diffusion of volatile SiF_y, and therefore impedes chemical etching.²⁴ Further, the fluorocarbon layer acts like a mask and prevents low-energy plasma particles from sputtering the surface of Si.²⁰ The ability of SiO₂ to react with carbon species in the polymer layer to produce volatile CO, CO₂, or COF₂ means that the etch rate of SiO₂ is inhibited to a much lesser extent by a fluorocarbon layer deposition.²² Further, the reaction between Si₃N₄ and the fluorocarbon layer is less effective than in the case of SiO₂, so that the etch rate of SiO₂ in a CHF₃ plasma is higher than that of Si₃N₄.^{20,22}

The trends observed in Figure 1 are quite different to the ones we have just discussed. These differences can be reconciled by accounting for the presence of O₂ in our plasma. Oxygen plays a major role in removing the protective polymer layer from the surfaces of Si and Si₃N₄.²⁰ Since the polymer-scavenging property of oxygen is only marginal for SiO₂ (already efficient at breaking down the fluorocarbon), addition of O₂ to the CHF₃

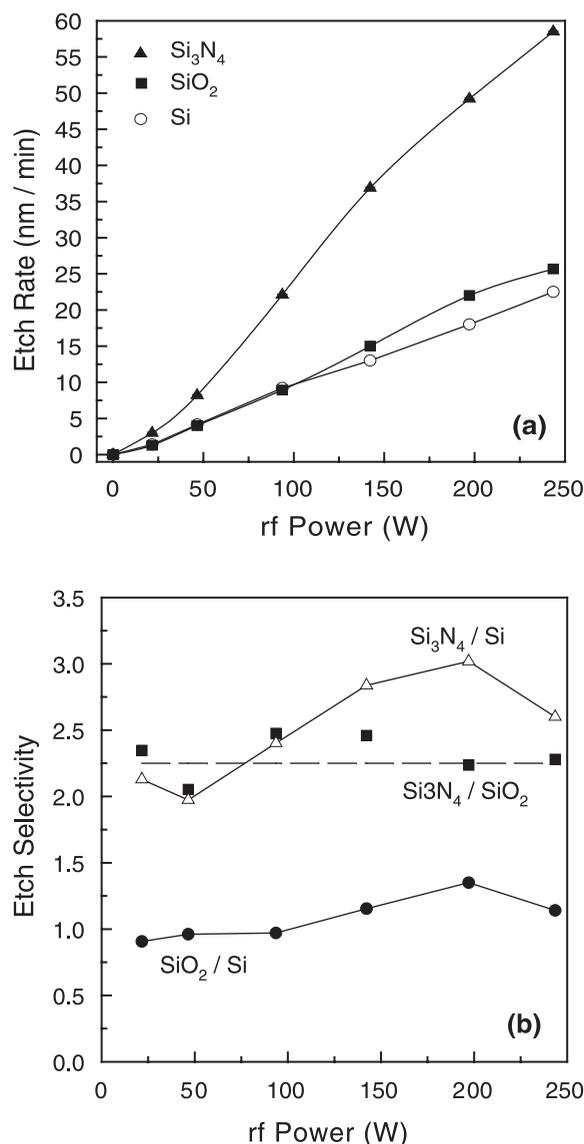


Figure 1. (a) Etch rates of SiO₂, Si₃N₄, and Si, and (b) etch selectivities as a function of rf power

plasma enhances the etch rate of both Si and Si₃N₄ relative to SiO₂. The effect can be expected to be more pronounced for Si₃N₄ than for Si because the steady-state thickness of the polymer layer is thinner on Si₃N₄ than on Si.²¹ Figure 1a shows that the change in the etch rate of Si₃N₄ and SiO₂ follow similar trends with increasing rf power. This makes the etch selectivity between the two dielectric fairly independent of rf power (Figure 1b).

As mentioned earlier in the introduction, RIE is achieved by a combination of chemical and physical (sputtering) etching. In RIE, the dc bias generated on the bottom electrode is coupled with the rf power, so that purely chemical etching cannot be separated from ion-induced chemical etching or chemical sputtering. Further, the energy threshold for ion-induced chemical etching is much lower than that for pure physical sputtering. The dc bias, and hence the energy of ions bombarding the exposed surfaces, increase with the increasing rf power. In order to establish the relative importance of chemical and physical sputtering, it is more appropriate to plot the etch rates in Figure 1 as a function of dc bias generated on the lower electrode during etching (Figure 2). Two

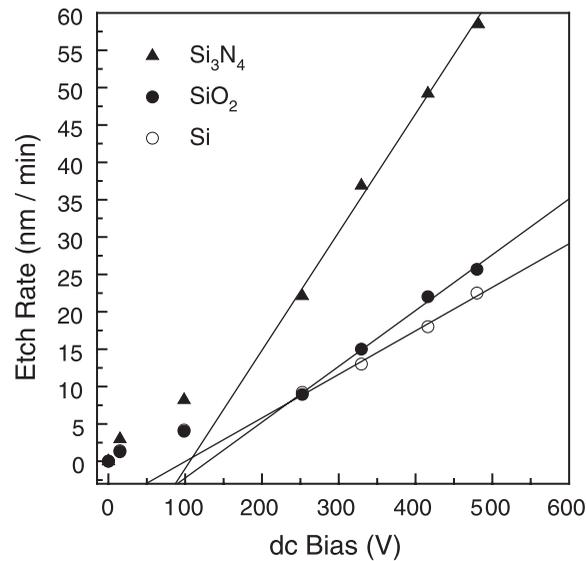


Figure 2. Etch rates of SiO₂, Si₃N₄, and Si as a function of the sample dc bias

etch rate regimes, A and B, can be identified in Figure 2. Below 100 V (i.e., regime A), the etch rates are relatively low, and this regime can be associated with predominantly chemical etching. Above 100 V (i.e., regime B), the effect of physical sputtering in the etch process becomes more significant as evidenced by the linear increase in etch rate with dc bias (proportional to energy of ions bombarding the surface).²⁶ In regime B, ion bombardment becomes more efficient so that the chemical reaction leading to desorption (i.e., removal) of the volatile species is promoted. It is worth pointing out that the chemical sputtering is mechanistically complicated and that a quantitative theory will have to include a plethora of phenomena including ballistic processes, the simultaneous deposition and etching of a polymer layer, chemical reaction in the near-surface region of ion bombarded layers, and desorption of volatile species.²⁷

RIE-INDUCED DAMAGE

This section looks at the damage created in Si through carrier lifetime measurements of reactive-ion-etched samples. In particular, we have investigated the time and power dependence of the lifetime modifications, as well as the isochronal annealing behavior of RIE-induced damage.

Time dependence of RIE

Figure 3a shows the variation of the carrier lifetime for sample B etched for different lengths of time at either 50 or 200 W. The effective lifetime, τ_{eff} , was measured at an excess carrier density of $\Delta n = 1 \times 10^{14}/\text{cm}^3$. Results are shown for the 150 Ω cm p-FZ samples because the effect of time was more clearly resolved due to the high initial effective lifetime. Etch times as short as 30 s produced reductions in τ_{eff} between two (50 W) and three (200 W) orders of magnitude, revealing the significant extent to which RIE adversely affects carrier lifetime. The results can be better analyzed by looking at the inverse of the effective lifetime, $1/\tau_{\text{eff}}$, which provides a measure of the defect concentration. Based on the Shockley–Read–Hall (SRH) theory of carrier generation and recombination at a discrete defect level in p-Si, the SRH lifetime can be expressed as:^{28,29}

$$\frac{1}{\tau_{\text{SRH}}^p} = \frac{N_A + \Delta n}{\tau_{p0}(n_1 + \Delta n) + \tau_{n0}(N_A + p_1 + \Delta n)} \quad (1)$$

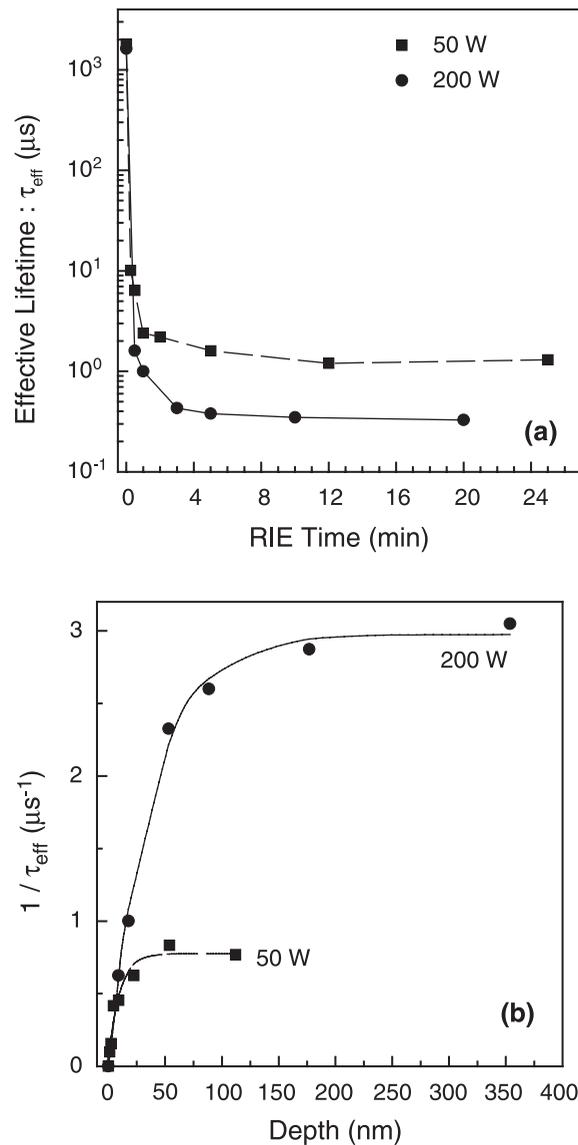


Figure 3. (a) The time-dependence of changes of minority carrier lifetime in sample $150 \Omega \text{ cm}$ p-Si for reactive ion etching (RIE) at 50 W (solid squares) or 200 W (solid circles). (b) Variation of the inverse of effective lifetime as a function of sample thickness etched by RIE. The depth scale was constructed using the values of etch rates in Figure 1

where, $\Delta n = \Delta p$ is the excess carrier density. The capture time constants τ_{n0} and τ_{p0} are related to the thermal velocity (v_{th}), the recombination center density (N_t), and capture-cross section (σ) via $\tau_{n0} = 1/(v_{\text{th}}\sigma_n N_t)$ and $\tau_{p0} = 1/(v_{\text{th}}\sigma_p N_t)$. It is clear from Equation 1 that $1/\tau_{\text{SRH}}$ is proportional to the density of the recombination center, N_t . The effective carrier lifetimes in the plasma-etched samples contain contributions from the RIE-induced defects, either in the near-surface region or in the bulk, and other recombination centers also present in the control samples. Figure 3a shows that, in all cases, the RIE-induced defects dominate the effective lifetimes. Hence, we can interpret the measured lifetimes as due solely to the presence of the defects caused by the RIE. Since the etch rate of Si is lower at 50 W than it is at 200 W (Figure 1a), it is more meaningful to compare the data for different rf powers on a depth scale. Figure 3b shows the variation of $1/\tau_{\text{eff}}$ as a function of

the thickness of Si etched at either 50 W or 200 W. Both curves exhibit similar shapes, with an initial increase in defect concentration leveling off for prolonged etching. In a previous study, we have shown that the initial build up of defects in samples etched at 200 W is proportional to time.³⁰ The shape of the curves in Figure 3b can be explained by considering the two competing processes involved in ion-induced chemical etching of Si. The energetic ions that bombard the Si generate defects below its surface. Initially, this process dominates the chemical sputtering process leading to the build up of damage (or defects) below the surface. In turn, the damaged layer favors the chemical reaction between Si and F radicals (and ions) to produce the volatile species (SiF_4) that desorb from the surface. This action results in the partial removal of the bombardment-induced damaged layer. For sufficiently long etching, an equilibrium is reached between ion-bombardment induced damage and ion-induced chemical etching, and this is observed as a plateau in Figure 3b. Since the desorption of volatile etch compounds is most effective within the first few monolayers of the substrate, the equilibration time (and therefore depth) depends on the penetration depth of energetic ions—that is, the energy of ions. The ion energy influences both the thickness of the damaged layer (penetration depth) and the extent of the damage (energy deposited in recoils). For fluorine ions, the penetration depth and number of vacancies produced per ion, calculated from TRIM simulations,³¹ are 1.1 nm and 1.4 vacancies/ion, and 2.4 nm and 6.6 vacancies/ion for RIE at 50 W (99 V) and 200 W (416 V), respectively. The absolute values of vacancies created per ion should be treated with caution since TRIM code does not account for Frenkel pair recombination. Since the production of defects and damage removal become spatially separated for higher dc biases (i.e., higher rf power), the equilibration depth increases accordingly as shown in Figure 3b.

Power dependence of minority carrier lifetime change

The variation of carrier lifetime was measured for the 150 Ω cm p-FZ and the 100 Ω cm n-FZ samples as a function of rf power as shown in Figure 4 for $\Delta n = 1 \times 10^{14}/\text{cm}^3$. Samples were etched simultaneously for 30 s, which corresponds to the maximum over-etch time for dielectric layers deposited on our Si substrates as part of the novel solar cell fabrication process mentioned earlier. Consequently, the carrier lifetimes do not reflect the steady-state concentrations of defects at the different rf powers. The minority carrier lifetimes in reactive ion etched n- and p-type Si are similar. We have determined the doping concentration of the high-resistivity n- and p-type samples through dark conductance measurements. The doping concentrations have been calculated to be

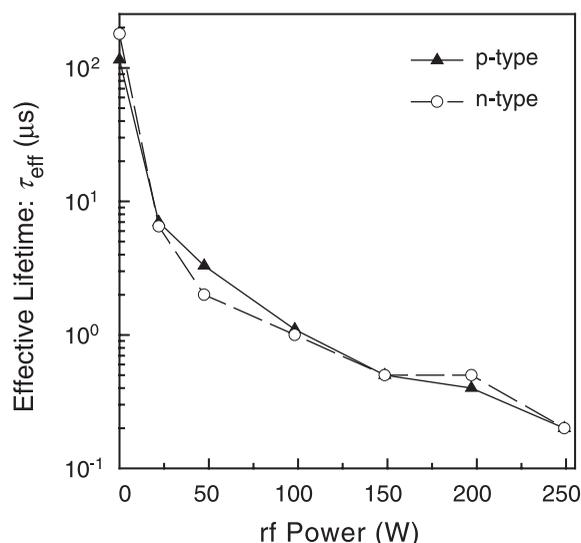


Figure 4. Variation of effective lifetime as a function of rf power for n- and p-type FZ Si. The data points are for the high-resistivity samples that have the similar doping concentration

$6 \times 10^{13}/\text{cm}^3$ and $3.5 \times 10^{13}/\text{cm}^3$ for the p- and n-type wafers, respectively. With a relative uncertainty of 10% attached to these values, and with some further variations expected between wafers from the same ingot, we may conclude that $N_A \approx N_D$ for the high-resistivity wafers. This observation is important since it reveals that, should a single deep level defect be responsible for the lifetime changes, the minority and majority carrier capture cross-sections of the defect should also be similar when $p_0 = n_0$ or $N_A = N_D$.³² The fact that $\sigma_n = \sigma_p$ is quite useful since DLTS provides only the majority carrier capture cross-section, and this will be discussed in more details later.

Isochronal annealing behavior of an etched sample

The post-RIE diffusion that we have used to prepare samples for lifetime measurements is of technological importance, since it mimics a high-temperature device processing step. It is also important to understand the behavior of plasma etched samples upon annealing at lower temperatures. For instance, etching dielectric layer through to the Si substrate could be used to selectively define areas for metallization towards the end of the device fabrication process. Typically, the metal contacts are then sintered at modest temperatures ranging between 350 and 450°C. Figure 5 shows the variation of minority carrier lifetime (for $\Delta n = 1 \times 10^{15}/\text{cm}^3$) as a function of post-RIE temperature for 1 Ω cm p-FZ samples. In each case, the surfaces of the samples were passivated with PECVD SiN:H. Similar results were obtained for the 150 Ω cm p-FZ samples (not shown). The control samples showed a gradual reduction in minority carrier lifetime with the increasing temperature above 400°C. The same trend is observed in the samples subject to RIE at 200 W for 10 s, with the improvement in lifetime following annealing at 400°C being more pronounced. The reason for the degradation in lifetime of the control samples at the higher annealing temperature is not clear to us at present. We can, however, exclude the influence of iron contamination in our annealed samples. This is evidenced by the similar values of minority carrier lifetime in samples before and after light soaking as shown in Figure 5.³³ One encouraging result from Figure 5 is the improvement in lifetime following annealing at 400°C, which is promising for the use of RIE in defining areas for subsequent metallization. This partial recovery is consistent with RIE-induced defect annealing. At this stage we speculate that the lifetime degradation in the plasma exposed samples annealed at the higher temperatures may be due to the formation of secondary defects arising from interactions between defects that are created by RIE.

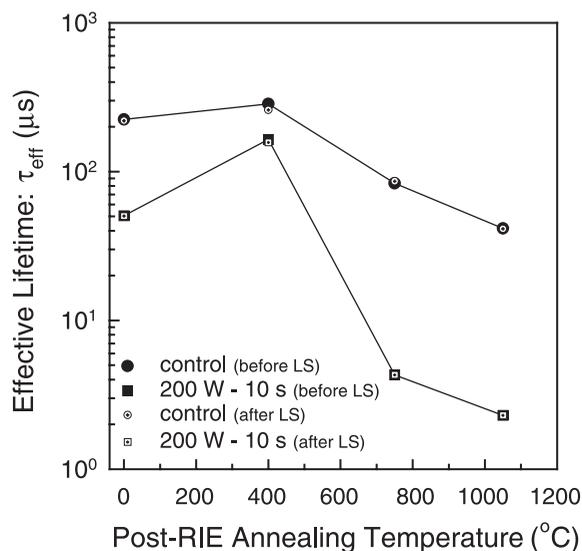


Figure 5. Isochronal annealing behavior of sample A following RIE at 200 W for 10 s. The data points shown as solid and crossed symbols were measured before and after light-soaking (LS), respectively

MODELING THE INJECTION-DEPENDENCE OF CARRIER LIFETIME USING ELECTRICAL PARAMETERS OBTAINED FROM DLTS

One limitation of QSSPC is that it is difficult to extract any direct information regarding the ‘signatures,’ such as energy position, E_t , in the band gap and capture cross-section, σ_a , of the recombination centers. One technique that can provide such information about defects is DLTS. Figure 6 shows the DLTS spectra from low-resistivity p- (circles) and n-type (solid triangles) Si. The combination of the three spectra reveal that only one discrete defect level B(0.32 eV), with $E_t = E_V + (0.32 \pm 0.02)$ eV and $\sigma_a \approx 4.2 \times 10^{-14}$ cm², was detected in reactive-ion-etched low-resistivity p-Si that had received phosphorous-diffusion and oxidation. The p-Si control sample contained a defect A(0.54 eV) with, $E_t = E_V + (0.54 \pm 0.02)$ eV, and $\sigma_a \approx 8.5 \times 10^{-14}$ cm². DLTS is not capable of providing information on the structure of defects, and a common procedure to tentatively identify defects is to compare their electrical ‘signatures’ to those of defects previously identified in the literature. By comparing the ‘signatures’ of A(0.54 eV) and B(0.32 eV) with those of defects previously reported in the literature and by performing isochronal annealing experiments, we had tentatively assigned the defects to the B_i–B_s–H complex and a B_i-related defect, respectively.³⁰ However, the results presented here have shown that the defect responsible for lifetime degradation should be the same in both n- and p-type Si. Hence, the defect cannot be related to dopant atoms. Hence, our previous tentative assignment that B(0.32 eV) was related to B_i is shown not to be valid in this study.

We have used the ‘signature’ of B(0.32 eV) to model the injection dependent minority carrier lifetime measurements from selected n- and p-type samples. One important point to retain from our earlier discussion is that the capture cross-section ratio $k = \sigma_n/\sigma_p \approx 1$ for the defect responsible for lifetime degradation in samples that have received RIE. The benefits of knowing this fact are twofold. Firstly, it relieves us of the problem that DLTS provides a measure of only the majority carrier capture cross-section of a defect. Secondly, for any given sample resistivity, we only have to show simulations for either an n-type or a p-type sample (Figure 4). In order to calculate the so-called SRH densities n_1 and p_1 in Equation (1), we have used the value of $E_t + E_V = 0.315$ eV in Equation (2).

$$n_1 = N_C \exp\left(-\frac{E_C - E_t}{kT}\right), \quad p_1 = N_V \exp\left(-\frac{E_t - E_V}{kT}\right) \quad (2)$$

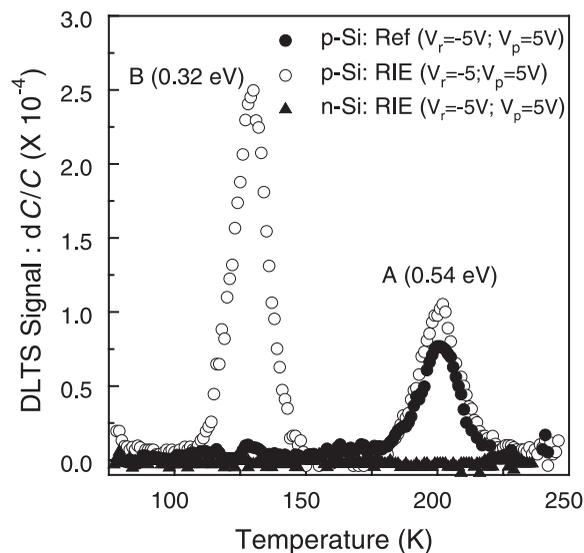


Figure 6. DLTS spectra taken from low-resistivity p- (circles) and n-type (solid triangles) Si that had received RIE. No defect peaks are seen in the spectrum from n-Si. A defect B(0.32 eV) is observed in the p-type sample after RIE

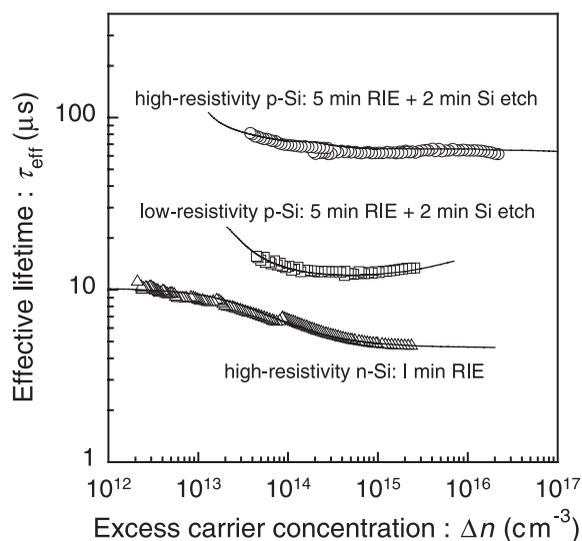


Figure 7. Modeling of the injection dependence of the minority carrier lifetimes in selected plasma-etched samples. Details of sample types and their processing are shown in the legends. The effect of minority carrier trapping centers is included in modeling as shown by the upward curves in low-injection

E_C and E_V are the energies of the conduction and valence band edges, and N_C and N_V are the effective densities of states in the conduction and the valence band, respectively. For completeness, we have included Auger recombination, which impacts at high excess carrier densities, in the modeling procedure.³⁴ Our methodology also allows the effect of minority carrier trapping, which may become pronounced in the low carrier injection regime, to be simulated.³⁵ The latter phenomenon may give rise to an apparent increase in effective lifetime in low-injection due to the temporary trapping of minority carriers followed by their subsequent release.

The solid lines in Figure 7 demonstrate that the experimental data points (open symbols) can be adequately simulated following the SRH formalism and using the ‘signature’ of B(0.32 eV). In simulations we have used $\sigma_n = 1 \times 10^{-15} \text{ cm}^2$, while σ_p was varied between 1×10^{-15} and $1.2 \times 10^{-15} \text{ cm}^2$. However, this observation has to be qualified. Firstly, there are large uncertainties associated with the capture cross-section used in this study. Consequently, the defect concentrations used in simulations do not necessarily correlate with those estimated from DLTS measurements for the low-resistivity p-Si sample. Further, it is pointed out that other combinations of E_t and σ_a may also provide reasonable fits to the experimental data, since Equation (1) does not have a unique solution. Nevertheless, the simulations in Figure 7 at least show that an energy level of 0.32 eV is not *inconsistent* with the measured injection dependence of minority carrier lifetime in samples that received RIE.

CONCLUSION

We have measured the etch rates of SiO_2 , Si_3N_4 , and Si by reactive ion etching in CHF_3/O_2 plasma as a function of rf power. Further, we have investigated the changes in carrier lifetime caused by RIE in n- and p-type FZ Si. The two competing processes of damage accumulation and damage removal in ion-induced chemical etching of Si are revealed by studying the time dependence of RIE at fixed rf powers. An initial linear buildup of damage with time is followed by a steady-state regime wherein defect creation is equal to damage removal by chemical sputtering. The rf power dependence of carrier lifetime is coupled to changes in the dc self-bias generated by the plasma. We have also shown that the electronic properties of a defect B(0.32 eV), together with the fact that the lifetime changes were similar in n-type and p-type samples of similar doping, to model the injection-dependence of the measured carrier lifetimes using the SRH formalism. Isochronal annealing experiments

showed that the lifetime of an RIE sample could be recovered partially by annealing at 400°C, but was reduced below its post-RIE value after annealing above 400°C. Annealing above 400°C also degraded the lifetime of control samples.

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